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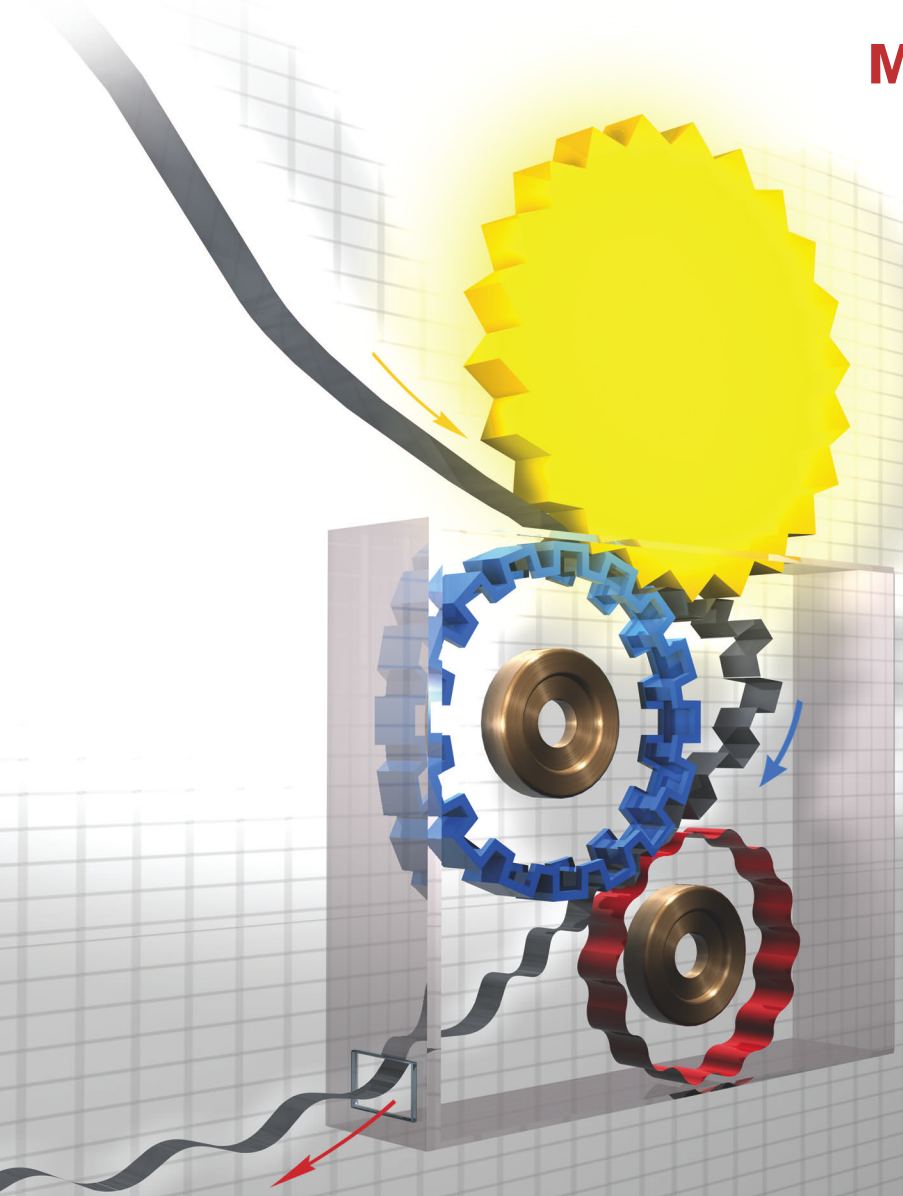

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innovation

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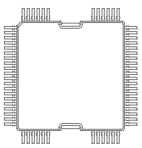
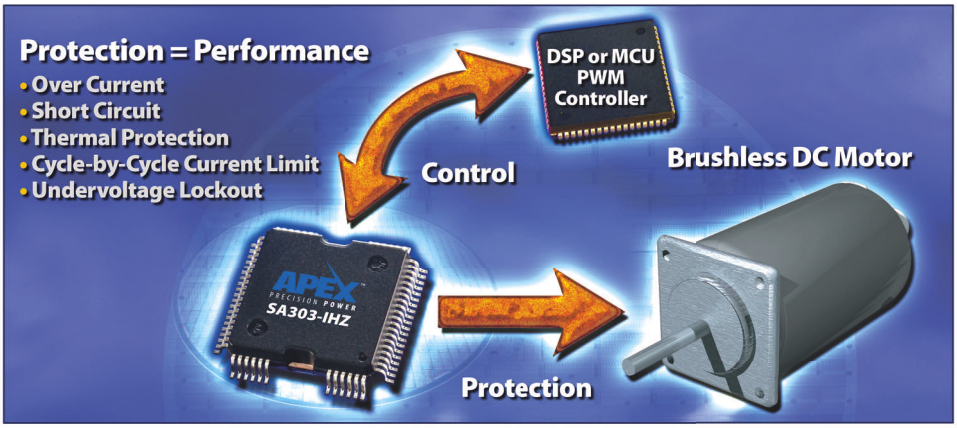


(actual footprint)



3 A, Three-Phase Motor Driver IC Uses Protection Features to Deliver Performance Gains

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  - Robotics
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  - Copiers, Fax Machines
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- Motor Drives – Aerospace, Military
  - Positioning Control
  - Aircraft Seating

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SA306-IHZ	Brushless DC Motor	5 A continuous 17 A PEAK	< 9 V to 60 V Single Supply	$9.90
SA306A-FHZ	Brushless DC Motor	8 A continuous 17 A PEAK	< 9 V to 60 V Single Supply	$12.85
SA53-IHZ	Brush DC Motor	3 A continuous 10 A Peak	10 V to 60 V Single Supply	$4.79
SA57-IHZ	Brush DC Motor	5 A continuous 17 A PEAK	< 9 V to 60 V Single Supply	$7.15
SA57A-FHZ	Brush DC Motor	8 A continuous 17 A PEAK	< 9 V to 60 V Single Supply	$9.05

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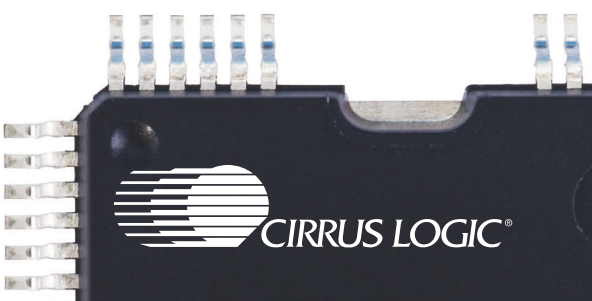

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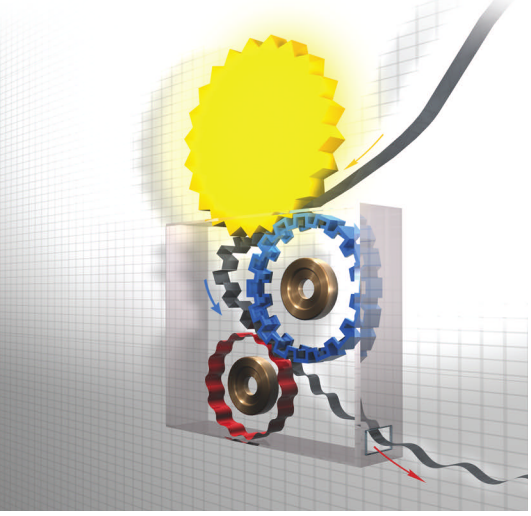

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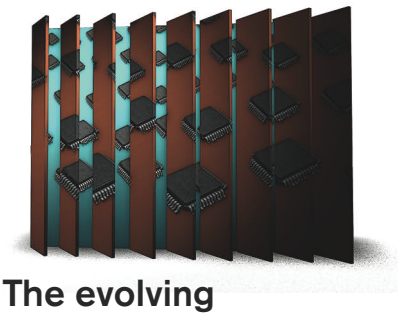
Microinverters and power optimizers

24 Alternative forms of power have become increasingly popular as utilities react to rising fuel prices and government mandates. Photovoltaic cells usually receive most of the attention as solar-energy cost drivers, but the ac/dc inverter design is equally important to overall system efficiency and cost.

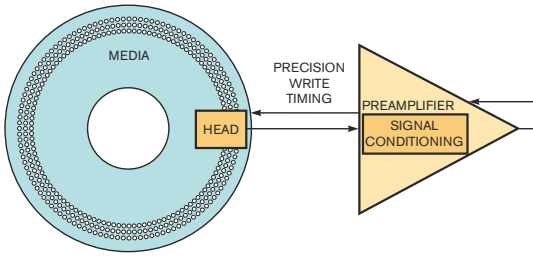
by Margery Conner, Technical Editor



The evolving landscape of digital signal processing

19 The continual evolution of microprocessors is one of the causes of a trend away from stand-alone DSPs.

by Robert Cravotta, Technical Editor



Preamplifier read-channel design addresses hard-drive goals

29 The hard-disk-drive industry is facing difficult challenges for increasing storage capacity and addressing cost, performance, power-consumption, and other important parameters. Jointly designing the media, head, flex, preamplifier, and read channel provides a good approach today and lays the foundation for future hard-drive generations.

by Harley Burger, LSI Corp

Taming inaccurate real-time clocks

33 An algorithm compensates for oscillator inaccuracies and adjusts to changes in the environment and aging.

by Rufus Michael Gnana and Nazmul Hoda, Ittiam Systems

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9 1G-sample/sec, 12-bit ADC works in base stations and instrumentation

10 Touch controller lets you ignore extra touches

10 Power-converter IC targets dimmable LEDs

11 Quad power-converter control chip uses PMBus

12 RF vector signal generator combines high throughput, low phase noise

13 PIC32 expands connectivity support

13 DSP is energy-efficient

13 Channel-simulator mode takes only seconds to determine ultralow BER

14 **Research Update:** Coated optical fibers promise uniquely flexible PV cells; An old material for batteries turns out to have another nature

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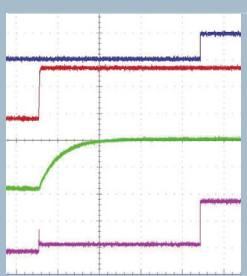


39 Precision tilt/fall detector consumes less than 1.5 mW

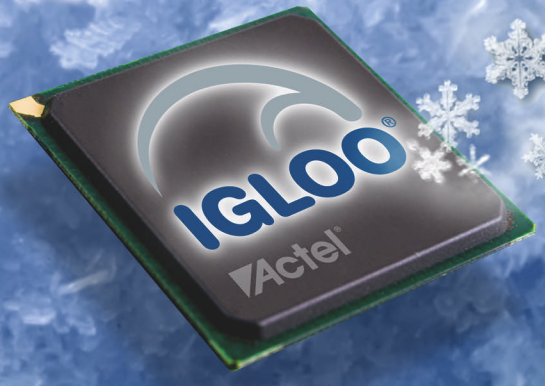
40 Reset an SOC only when power is ready

44 Circuit provides simpler power-supply-sequence testing

46 Inexpensive power switch includes submicrosecond circuit breaker

48 Create a DAC from a microcontroller's ADC

Cool it.



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●	●	●	Small Footprint	○	●	○
●	○	○	Logic Density	●	○	●
○	○	●	I/O to Logic Ratio	○	○	○
○	○	○	Speed	●	●	●
○	○	○	Low Cost	●	●	●

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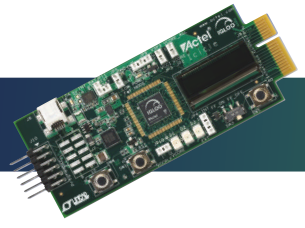

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→www.edn.com/article/CA6707615

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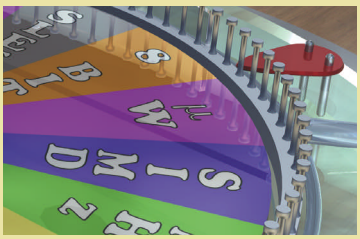

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BY BRIAN DIPERT, SENIOR TECHNICAL EDITOR

Call me unconvinced by USB 3.0

At September's IDF (Intel Developer Forum) in San Francisco, Steve Roux, senior strategic-business-development manager for USB (Universal Serial Bus) technologies at NEC Electronics, touted the benefits of Superspeed Version 3 of the USB specification, which is looming on the horizon. Judging from both company announcements and customer implementations, NEC is one of the notable Version 3 USB leaders in both stand-alone SOCs (systems on chips) and IP (intellectual-property)-core capability from its ASIC division.

Plenty of folks in the USB Pavilion at IDF were eager to chat about USB 3.0's 5-Gbps bandwidth potential and the extensive assortment of applications it will supposedly unleash.

Call me skeptical, at least in the short term. Consider first the viability of the 5-Gbps USB 3.0 performance claim. Anyone who has done USB 2.0 development and benchmarking will likely attest that real-life implementations don't come close to the technology's 480-Mbps potential. One reason for this disparity is that USB, unlike, say, IEEE-1394 FireWire, relies heavily on regular CPU intervention from transaction arbitration and scheduling standpoints. Other tasks can distract the CPU, making it less likely that the USB protocol's potential will translate into reality, even discounting the effects of multiple USB peripherals contending for common bus bandwidth. The other key reason for the disparity involves the applications themselves.

Mass-storage interfaces—as external hard-disk drives and as tethers to solid-state and magnetic storage within cameras and other devices—are obvious, popular uses for USB. A previous article compares eSATA (external

serial-advanced-technology attachment), 400- and 800-Mbps IEEE-1394, and USB 2.0 (see "Interface overkill?" *EDN*, May 10, 2007, pg 48, www.edn.com/article/CA6437950). The article describes how USB 2.0 notably undershoots the performance potential of both hard-disk and solid-state drives. Other higher-speed interface alternatives, such as HDMI (high-definition-multimedia interface) for digital videocameras, also exist for applications that demand higher speed than USB 2.0 can deliver. The cost constraints may preclude mass-market adoption of multi-interface designs, however. This same pricing pressure also means that USB 3.0 must achieve cost parity with USB 2.0 before the generational evolution will occur in earnest. At any rate, initial USB 2.0-versus-3.0 performance statistics were underwhelming, although more recent studies have garnered more promising results.

NEC's Roux also pitched such USB 3.0 applications as computer synchronization of PDAs (personal digital assistants), smartphones, portable multimedia devices, and the like, which currently operate at low speeds. In my experience, though, they're not notably faster over USB 2.0 than over USB 1.1, which suggests that the content-reconciliation routines running on both the computer and the tethered client—not the tether itself—are causing the bottleneck. As such, I doubt that USB 3.0 will make further discernible performance improvements. Speed aside, I wonder how much longer physical-wire tethering will be relevant. Don't consumers prefer reliable wireless tethering, either client to client or through a "cloud" intermediary server, and over Bluetooth, Wi-Fi, or a proprietary protocol?

Intel has remained mum on its USB 3.0-implementation schedule for its core-logic chip sets. As history shows, though, Intel's embrace of core logic is key to interface success. Rumors on the show floor at IDF suggested that Intel's adoption of USB 3.0 might slip to 2011 or later, and subsequent comments from both Intel's customers and its competitors bolster that contention. I also wonder whether Intel plans for even faster Light Peak technology, an optical-interconnect cable for PCs and mobile devices, to effectively obsolete USB 3.0.

Kudos to companies such as NEC for securing embryonic USB 3.0 design wins in both system boards and add-in cards. As with IEEE-1394, the IC sales will likely—at least at first—be profitable on a per-unit basis. As with IEEE-1394, however, they'll remain minuscule in volume unless manufacturers successfully address compelling application benefits and broad adoption. EDN

Contact me at bdipert@reedbusiness.com.

Read more at www.edn.com/blog/400000040/post/1560050356.html.

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INNOVATIONS & INNOVATORS

1G-sample/sec, 12-bit ADC works in base stations and instrumentation

Targeting applications in wireless-communications, defense, and test-and-measurement equipment, Texas Instruments recently announced the 12-bit, 1G-sample/sec ADS5400 ADC with 2.1-GHz input bandwidth. You can adjust the device's gain, offset, and phase to interleave two or more ADCs to create a multigigabit-sample/second digitizer or to balance two ADCs in an I/Q (in-phase/quadrature) wireless receiver. You can select between single- or dual-bus DDR LVDS (low-voltage-differential-signaling) outputs.

The device offers an SNR (signal-to-noise ratio) of 59 dBFS (decibels below full-scale) and 75 dBc (decibels referenced to the carrier) SFDR (spurious-free dynamic range) in the first Nyquist frequency range. For intermediate frequencies beyond 1000 MHz, the SNR is 58 dBFS, and the SFDR is 70 dBc. The device has buffered analog inputs and an internal sample-and-hold circuit.

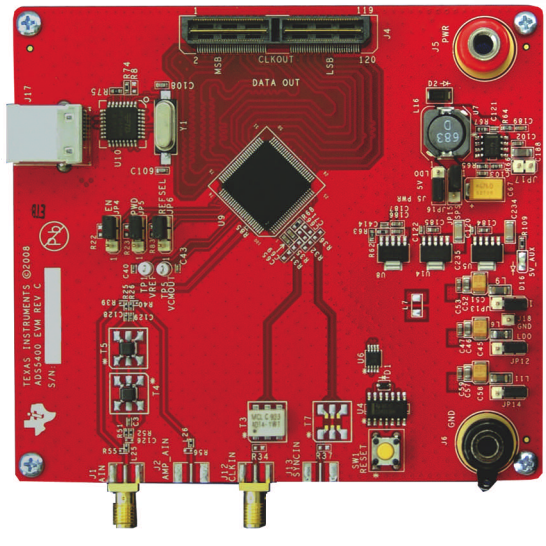
The ADS5400 comes in a 100-pin 16×16-mm TQFP package, operates over −40 to 85°C, and sells for $775 (1000). Samples and an evaluation board that is compatible with TI's TSW1200EVM digital-capture card are available now.**—by Paul Rako**

▷**Texas Instruments**, www.ti.com.

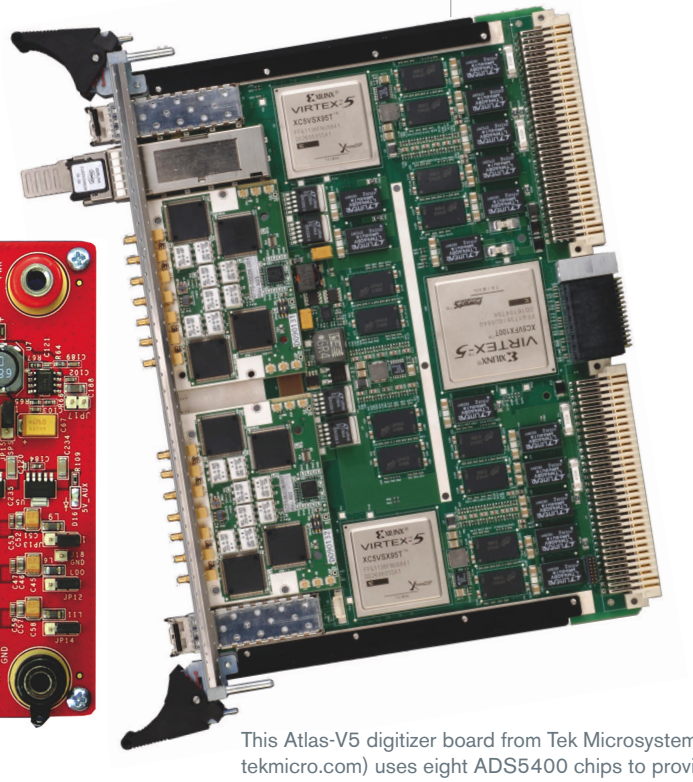
FEEDBACK LOOP

"Will the machines eventually take over? Nope. People have wants; machines want nothing."

—Hardware architect David Wyland, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6694951. Add your comments.



The evaluation board for TI's ADS5400 ADC allows you to assess the unit's performance.



This Atlas-V5 digitizer board from Tek Microsystems (www.tekmicro.com) uses eight ADS5400 chips to provide fast digitization for applications such as beam forming, radar, military countermeasures, and wireless communications.

Touch controller lets you ignore extra touches

The mXT224 maXTouch touchscreen controller from Atmel combines the company's mutual capacitive sensors, a charge-transfer method of signal acquisition, and an Xmega microcontroller with bundled software to provide processing for handling an unlimited number of touches on a touchscreen. Mutual capacitance sensors avoid the ambiguity of multitouch positions that self-capacitance sensors experience by forming independent sensing nodes at each intersection of rows and columns over the display surface. At each intersection, the sensor emits a fixed number of mutually coupled voltage pulses along each set of row and column lines; this action causes a known current flow in the selected pair of lines. This sensing approach yields an SNR (signal-to-noise ratio) of 80-to-1, which enables the system to unambiguously manage multiple simultaneous touches and more accurately sense weak and adjacent signals with a refresh rate as high as 250 Hz.

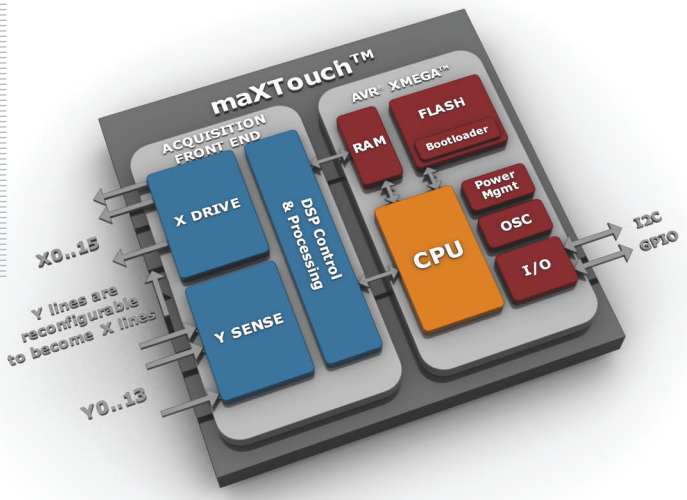
The integrated processor and bundled software provide additional processing for advanced noise-suppression algorithms for even more immunity to coupled-noise issues. Altogether, this approach enables the system to better identify and ignore unintended touches, such as when a user's hand overlaps the edge of the display while holding it or rests on the writing surface while using a stylus to provide a signature.

The mXT224 supports 224 X/Y sensing nodes and consumes less than 5 mW. It provides enough precision to support zoom, pinching, rotate, handwriting, and shape-recognition capability in screens as large as 10 in. You can use multiple mXT224 controllers together to provide smaller interspatial distances between touches on larger screens. The integrated single-cycle RISC AVR core includes two on-chip DSP engines that process the X and Y positions on the touchscreen. The system provides 16 X drive lines and 14 Y sense lines; you can reconfigure as many as four of the Y sense lines as X drive lines for a 20×10-line configuration.

The mXT224 is available now in a 5×5-mm BGA package and sells for $4.75 (1 million). The EVK-mXT224A evaluation kit, including a 4.3-in. touchscreen and a PCB (printed-circuit board) that connects to a PC over USB, is available now for $400. For more on these products, go to www.edn.com/article/CA6699917.

—by Robert Cravotta

▷**Atmel**, www.atmel.com.



The mXT224 encompasses the front-end signal-acquisition and postprocessing algorithms for multitouch systems in a single package.

POWER-CONVERTER IC TARGETS DIMMABLE LEDs

12.03.09

The large installed base of dimmable-lighting switches dictates that most new lighting technologies, including LED lights, should support dimming, and the myriad disparate specifications for dimming switches require these lights to meet a wide range of characteristics. Meeting both of those requirements, iWatt's new iW3610 ac/dc digital-power controller for dimmable LEDs includes intelligent wall-dimmer detection for both leading- and trailing-edge dimmers. It also detects an unsupported dimmer and turns off the light rather than self-destructing. The IC supports dimming from 2 to 100% and has an optimized dimming frequency of 900 Hz, so there is no visible flickering over the entire range.

The iW3610 provides ac/dc-power control for dimmable LED lights.

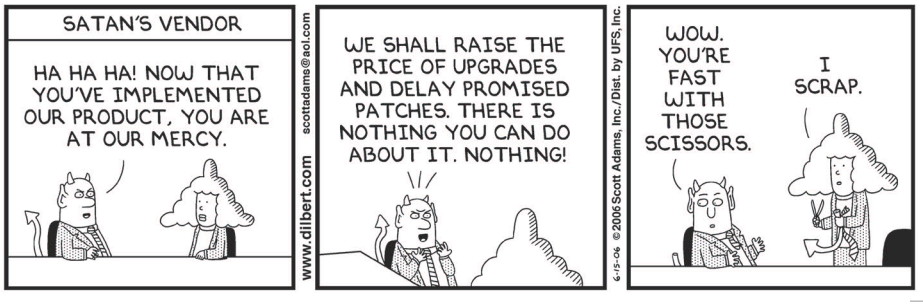
The 3610 uses primary-side regulation, eliminating the need for an optocoupler and sense resistor for dimmable LED lights of 40W or lower wattage. Another version, the iW3620, is similar to the 3610 but does not support dimming.

The 3620 has an internal switching frequency of 130 kHz and sells for 38 cents (1000); the 3610 sells for 98 cents (1000). For more, go to www.edn.com/article/CA6706827.

—by Margery Conner

▶**iWatt, www.iwatt.com.**

DILBERT By Scott Adams

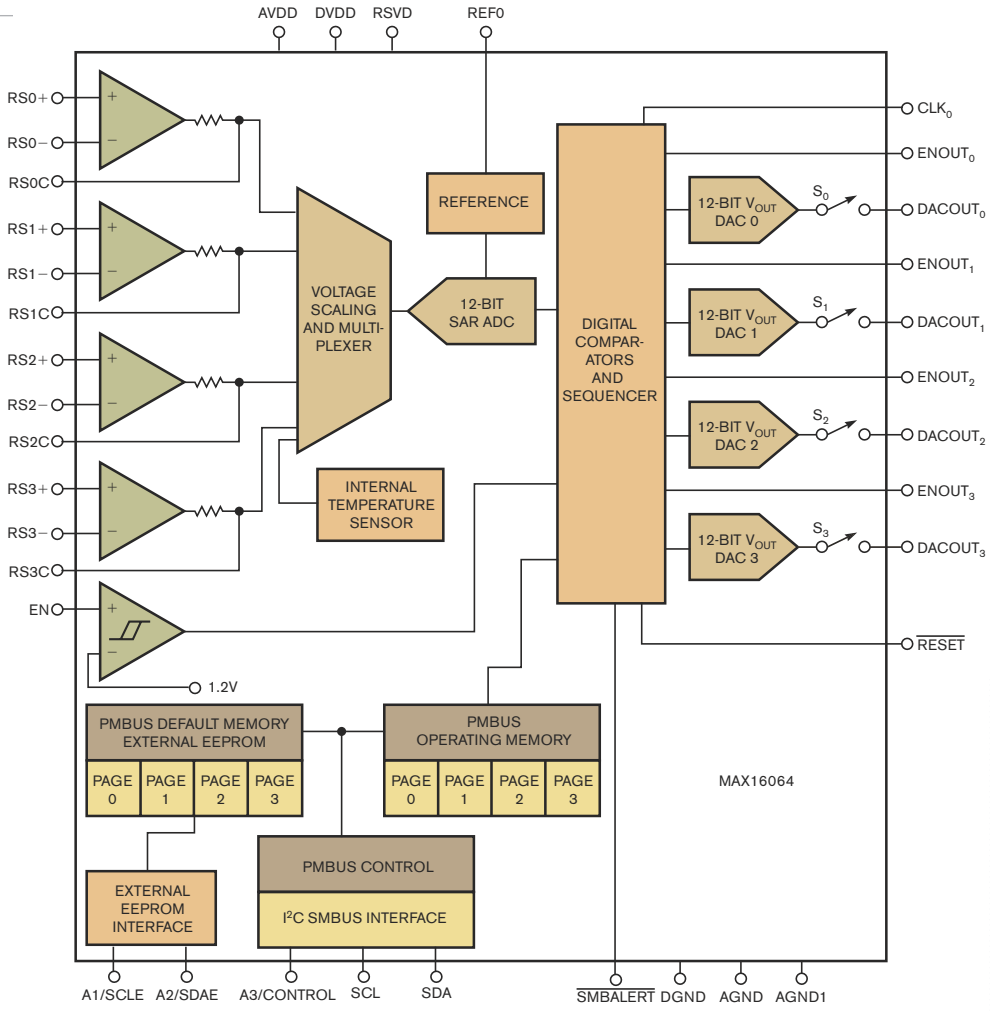


Quad power-converter-control chip uses PMBus

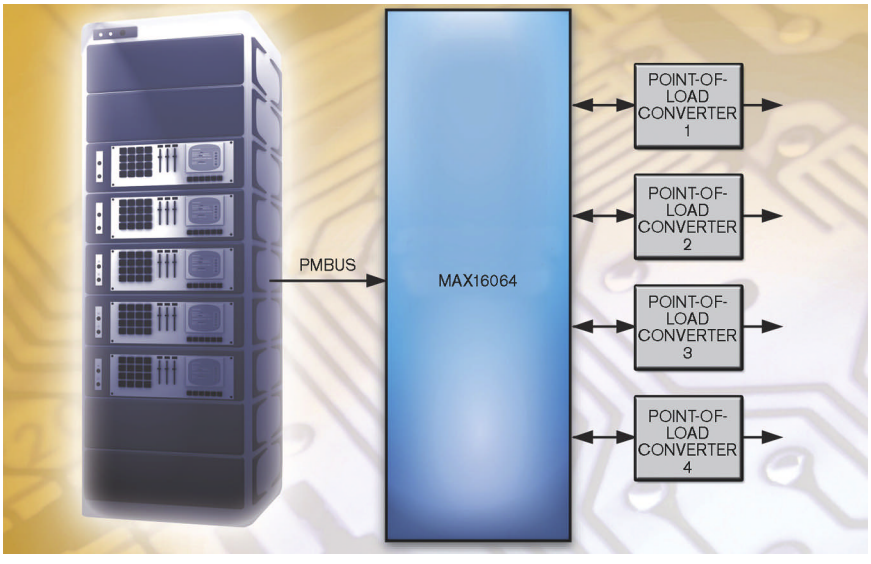
Maxim's new MAX16064 monitoring-and-control chip supervises four analog switching power converters. You communicate with the IC over the PMBus (power-management bus) to perform sequencing, monitoring, and margining of analog power supplies. The device controls output voltages with ±0.3% accuracy, and you can power it from 3 to 3.3V rails. Other features include an internal temperature sensor, a reset output, and an SMBus (system-management-bus) alert output. You can also store the chip's user-programmable registers in a low-cost external EEPROM. At power-up, the MAX16064 automatically retrieves the EEPROM data and loads the registers without requiring a system controller. Storing fault data in the external EEPROM also eases the identification and debugging of failures. The part features master/slave-clock options so that you can maintain accurate timing references across multiple devices.

Applications include high-reliability systems, such as servers, storage, base stations, routers, and networking equipment with multiple power supplies. The unit includes a GUI (graphical user interface) for implementing a digitally programmable power supply. The MAX16064 comes in a 6×6-mm, 36-pin TQFN package; operates in the −40 to +85°C range; and sells for $6.34 (1000).**—by Paul Rako**

▷**Maxim Integrated Products**, www.maxim-ic.com.



The Maxim MAX16064 controls four analog power supplies through the PMBus, providing digital-power benefits to analog-power systems.



The Maxim MAX16064 digital controller chip adds the benefits of digital power to analog converters.

RF vector signal generator combines high throughput, low phase noise

Keithley Instruments has upgraded its RF vector signal generator line with new capabilities that reduce signal-generation times and enhance signal quality. The instrument, which provides signal-generation-bandwidth options to 80 MHz and frequency ranges from 10 MHz to either 4 or 6 GHz, sells for $17,850 and $23,460, respectively.

A patent-pending technique, which ensures fast settling of phase-locked-loop synthesizers, allows the instrument to tune in 300 µsec or less to new frequencies in a DUT's (device under test's) operating band; competitive products typically require 600 µsec or longer. The unit allows switching of amplitudes in as little as 150 µsec compared with more than 500 µsec for competitive generators. This fast settling reduces the time required to test devices over their full power-handling range.

Because testing of devices that operate on multiple standards requires rapid switching among numerous complex signals, the unit's onboard arbitrary-waveform generator includes a 100M-sample memory that can hold large individual waveforms or multiple smaller ones. This deep memory combines with the instrument's speed-optimized list mode and a sequencer operating mode to support switching from one waveform to another within a single processor-clock cycle—even with waveforms that conform to different standards and employ different modulation schemes.

A direct link from the instrument's digital-signal-processing-circuit block to an external PC through a USB (Universal Serial Bus) 2.0 maximizes operating speed. In this high-speed desktop-control-panel operating mode, the external PC controls the instrument and acts as if it were the instrument's onboard-processor controller. This mode supports 100-Mbps transfers of signal files from the PC directly into the instrument's arbitrary-waveform memory and enables faster, simpler downloading of large files, such as streaming-video-test-signal files, signal files modified by channel models, and radar-profile files. With its high download speed and the manufacturer's application software, the unit can quickly perform dynamic-frequency-selection-conformance testing on WLAN (wireless local-area-network) access points, verifying a device's compliance with government and industry standards, which ensure that these transmissions do not interfere with radar signals, such as those for weather monitoring and air-traffic control. You can create waveform files offline and download them into the instrument's arbitrary-waveform memory using a USB memory stick or the unit's IEEE 488 or LAN interfaces. This transfer flexibility is convenient for those who create signal files with third-party tools, such as The MathWorks' (www.mathworks.com) Matlab.

> The unit allows switching of amplitudes in as little as 150 µsec.

Unlike competitive signal generators, which typically maximize either throughput or signal purity, the 2920A's design allows you to optimize whichever performance aspect is more critical in your application: High signal purity is essential when you create complex signals that conform to many wireless-communication standards. To ensure the quality of these signals, the 2920A-UPN (ultralow-phase-noise) option provides noise levels of less than or equal to −135 dBc/Hz at a 300-kHz offset from a 2-GHz carrier. This performance allows the generation of wideband-code-division-multiple-access signals with EVMs (error-vector magnitudes) of less than 0.85% of the signal amplitude. This option also permits the 2920A to generate 5.8-GHz, 40-MHz-bandwidth IEEE 802.11n WLAN signals with an EVM of less than −43 dB and WiMax signals with a residual relative constellation error of less than or equal to −43 dB. In addition, when you use the UPN option, the 2920A provides tuning as fast as 750 µsec.

The 2920A's wide signal range suits it to testing a broad spectrum of receivers and components. The 2920A-LAR (low-amplitude-range) option extends that range to allow the generator to output signals of −130 to +13 dBm. The unit's accuracy, repeatability, and stability allow you to set narrow limit bands in your test protocols. Absolute amplitude accuracy to 3 GHz is ±0.6 dB maximum, or ±0.3 dB typical, from −110 to +13 dBm. Relative amplitude accuracy, or linearity, is ±0.05 dB, and amplitude repeatability is ±0.05dB.

With the manufacturer's SignalMeister RF-communications-test-tool-kit software and Model 2820A vector signal analyzer, it can easily generate and analyze MIMO (multiple-input/multiple-output) signals. With signal personalities that the software provides, the 2920A can not only generate pure signals but also replicate impaired signals for in-depth receiver characterization. For more on this product, go to www.edn.com/article/CA6700416.

—by Dan Strassberg

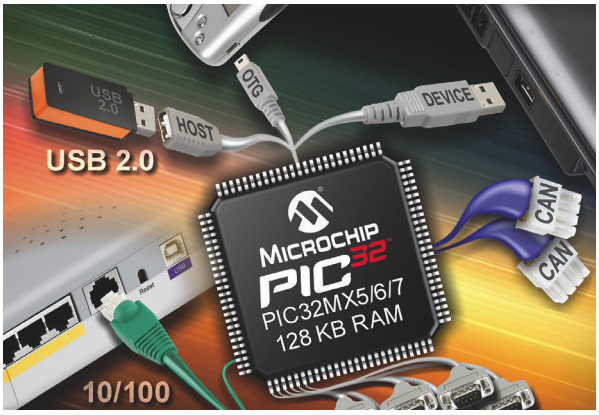
▷**Keithley Instruments Inc**, www.keithley.com/products.

The cost-effective 2920A RF signal generator does not force trade-offs between accuracy for component evaluation in R&D and speed for production test.

PIC32 expands connectivity support

Microchip Technology's PIC32MX5/6/7-family chips expand the connectivity support of PIC32 processors to cover 10/100-Mbps Ethernet; CAN (controller-area-network) 2.0b; and USB (Universal Serial Bus) host, device, and OTG (On-The-Go) peripherals. The company offers free TCP/IP (Transmission Control Protocol/Internet Protocol) and USB host- and device-software stacks, including source code, for these families. The 100-Mbps Ethernet MAC (media-access controller) uses an RMII/MII (reduced media-independent interface/media-independent interface) and includes a unique factory-preprogrammed Ethernet MAC address.

The CAN2.0b controllers use system RAM for storing as many as 1024 messages in 32 buffers with as many as 32 filters and four filter masks. Additional available software includes support for AES (Advanced Encryption Standard), multiple file systems, graphics, and audio libraries.



Microchip's PIC32MX5/6/7 ICs cover Ethernet, CAN, and USB connectivity.

The 80-MHz, 32-bit processors include as much as 128 kbytes of RAM, six UARTs (universal-asynchronous-transmitter/receiver) interfaces, five I²C (inter-integrated-circuit) interfaces, and four SPI (serial-peripheral-interface) ports.

The three new PIC32-MX5/6/7 families are available for sampling, and prices range from $4.73 to $6.55 (10,000). Package options include 100-pin TQFP and BGA packages and 64-pin TQFP and QFN packages.

The PIC32MX5/6/7 families are pin-compatible with the PIC32 and 16-bit PIC24F USB devices. Starter kits include the $72 DM320004 PIC32 Ethernet starter kit and the $55 DM320003-2 PIC32 USB II starter kit. Owners of the DM240001 Explorer 16 development board can purchase the $25 MJA320003 plug-in module for development with the new PIC32MX5/6/7 families.**—by Robert Cravotta**

▷**Microchip**, www.microchip.com.

Channel-simulator mode takes only seconds to determine ultralow BER

Agilent Technologies has introduced a statistical mode for its signal-integrity channel-simulator tool. The mode, part of Agilent's ADS (Advanced Design System) 2009 Update 1, supports the design and verification of today's high-speed, chip-to-chip data links in most consumer and enterprise digital products—from laptop computers and data-center servers to telecommunication switching centers and Internet routers.

The simulator eliminates the need for costly and time-consuming prototype iterations and allows designers to perform simulations using circuit-level models that they can then verify against measured data and EM (electromagnetic) simulation of the layout. ADS 2009 Update 1 also features a BER contour and bathtub display, equalizer support with automatic tap optimization, an eye-mask utility with automatic violation checking, the ability to check crosstalk with aggressors at different data rates, a memory-bus-compliance tool for the DDR3 standard, ECL (emitter-coupled-logic) models that comply with the IBIS (input/output-buffer-information specification), and a time-domain-reflectometry tool.

The Agilent ADS 2009 Update 1 is now available. The base price for the new channel-simulator mode is $28,000. For more information on this product, go to www.edn.com/article/CA6702836.**—by Rick Nelson**

▷**Agilent Technologies**, www.agilent.com/find/signal-integrity.

DSP IS ENERGY-EFFICIENCT

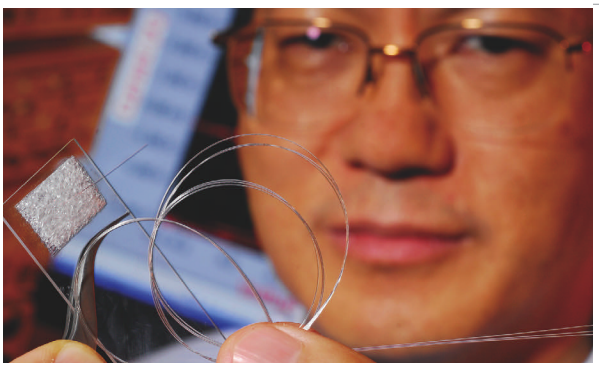
Texas Instruments' new six-core TMS320C6472 DSP boasts a 3.68W power-use sweet spot when operating all six cores at 500 MHz with 80% usage. The cores support 625- and 700-MHz operation with a trade-off of energy efficiency at the 500-MHz operation point. The device includes 4.8 Mbytes of L1 and L2 memory partitioned so that each core has a dedicated portion of the memory as well as access to 768 kbytes of shared L2 program/data memory. The shared-memory controller provides no hardware-based coherency support, so applications requiring coherency require software management.

Connectivity peripherals include GbE (gigabit Ethernet), Serial RapidIO, DDR2, a telecom-serial-interface port, a host-port interface, Utopia, I²C (inter-integrated circuit), and GPIO (general-purpose input/output). These devices target high-end industrial, test-and-measurement, communication, medical-imaging, high-end imaging and video, and blade-server designs.

The TMS320C6472 is available now at prices starting at $140 (1000). The TMDXEVM6472 evaluation module is available for $349. For more on this product, go to www.edn.com/article/CA6705855.

—by Robert Cravotta

▶Texas Instruments, www.ti.com.



Zhong Lin Wang holds a prototype 3-D solar cell that could allow designers to locate PV systems away from rooftops.

RESEARCH UPDATE

BY RON WILSON

Coated optical fibers promise uniquely flexible PV cells

One of the big practical issues with silicon solar cells is where to put them. Their conversion surface is also their collecting surface, so you end up with a huge flat panel facing the sun. This scenario limits the configurations in which designers can deploy the panels.

Now, researchers at the Georgia Institute of Technology have found an alternative. By coating an optical fiber with a nanostructured, dye-sensitized PV (photovoltaic) coating, the researchers have created a device in which conversion takes place over a dense nanowire fur all along the surface of the fiber, giving a conversion surface far greater than the collecting surface's area.

To form the structure, Zhong Lin Wang, Georgia Tech Regents Professor of materials science and engineering, and his team first strip the cladding from a communications-grade quartz fiber. They then apply a conductive coating and a seed layer of zinc oxide to the wall of the fiber. They grow zinc-oxide nanowires on the prepared surface with established techniques, ending up with a fiber surrounded by a fur of nanowires with an enormous total surface area. The researchers then coat the nanowires with dye-sensitized PV material, immerse the fiber in liquid electrolyte to collect the current from the PV reaction, and point the end of the fiber at the sun or focus lighting into the fiber with external optics.

Wang says the structure's high saturation intensity makes optical concentration productive. Once light enters the unclad fiber, some light passes through the wall into the nanowires at each reflection along the inside wall and thence into the huge area of PV material. Wang and his team have demonstrated 20-cm fibers and 3.3% efficiency; switching to titanium oxide and improving charge collection could increase conversion efficiency to perhaps 8%.

▷**Georgia Tech**, www.gatech.edu.

AN OLD MATERIAL FOR BATTERIES TURNS OUT TO HAVE ANOTHER NATURE

A team from Johns Hopkins University recently found that a nonsemiconductor that has long found use as a conductor turns out also to be, in a different orientation, an insulator, with properties useful in constructing MOSFETs (Reference 1). The material, solution-deposited beta alumina, forms when aluminum oxide from solution forms solid layers of crystals.

Howard E Katz, professor of materials science and engineering at Johns Hopkins, explains that, because the material forms from solution, it is easy to lay down in arbitrary patterns. Heating the deposited material to 400°C causes the formation of sodium beta alumina, a hard, transparent film with the mobile sodium ions still trapped between planes of aluminum oxide. These characteristics make the film compatible with applications on the surface of flat-panel displays, for example.

The familiar conductor conducts only when parallel to the plane of the film. Perpendicular to this plane, the material acts as an insulator. Further, if you apply a voltage perpendicular to the film, the voltage causes the ions trapped between layers of alumina to shift, polarizing the material. This polarization results in a dielectric constant (k) of 200–about 50 times that of silicon dioxide.

The team has employed sodium beta-alumina films to fabricate FETs on a variety of semiconductor substrates, including silicon and indium-zinc oxide. The transistors display low-voltage operation, the ability to operate into low-megahertz frequencies, transparency, and flexibility.

▶Johns Hopkins, www.jhu.edu.

Howard E Katz adjusts probes for testing electronic devices (photo courtesy Will Kirk, Homewoodphoto.jhu.edu).

REFERENCE

1 Pal, Bhola N, Bal Mukund Dhar, Kevin C See, and Howard E Katz, "Solution-deposited sodium beta-alumina gate dielectrics for low-voltage and transparent field-effect transistors," *Nature Materials*, November 2009, Volume 8, No. 11, pg 898, www.nature.com/nmat/journal/v8/n11/abs/nmat2560.html.

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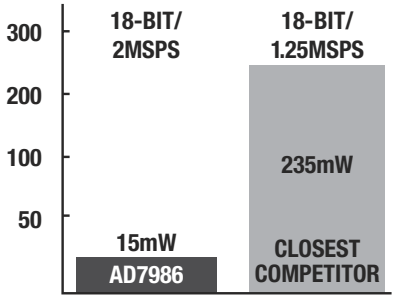

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ANALOG DEVICES

BY HOWARD JOHNSON, PhD

Making Gaussian edges

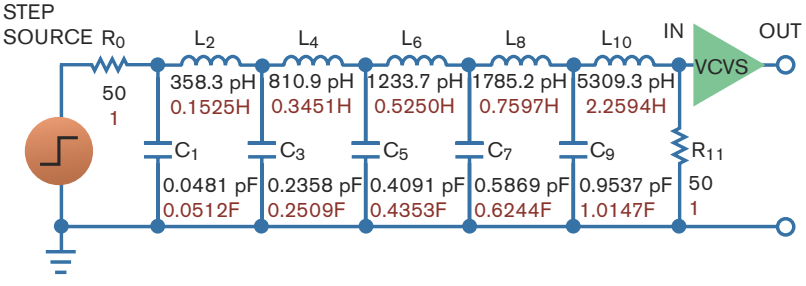
The analog-filter network in **Figure 1** converts each input step into a smooth, Gaussian-shaped rising and falling edge. When simulating high-speed systems in Spice, you can use this filter network instead of PWL (piecewise-linear) edge-shaping because it better represents how real signals behave.

The analog filter comes from Anatol I Zverev's *Handbook of Filter Synthesis*, a classic compendium of passive-filter designs (**Reference 1**). The book lists circuits for implementing many types of filters, including approximations of the Gaussian filter. The approximation is not exact because an actual, perfect, Gaussian response would have an infinitely long precursor. The author derives the filter approximation as a 10th-order truncation of the Taylor series expansion for the square of a perfect Gaussian-network function. He assumes ideal components with no significant parasitic effects.

The analog-filter network better represents how real signals behave.

Zverev specifies a current-source driver for the filter and shunts the current source with resistor R_0. **Figure 1** drives the circuit differently. It uses a voltage source that connects in series with R_0. Either approach produces a driver with an output impedance of 50Ω. Using a voltage source ensures that the circuit's output amplitude will be precisely half the voltage source's amplitude.

The circuit values in black in **Figure 1** differ from the original circuit values in Zverev's book, which the **figure** shows in red. The author designed his circuit for an impedance level of 1Ω. **Figure 1** scales that impedance to a more commonly accepted value of 50Ω. It does so by multiplying the book's resistances and inductances by 50 and dividing the capacitances by 50.



NOTE: THE COMPONENT VALUES IN RED ARE THOSE IN THE ORIGINAL CIRCUIT IN REFERENCE 1.

Figure 1 This 10-pole network approximates a Gaussian filter with a 10 to 90% rise and fall time of 100 psec.

The 3-dB frequency of Zverev's original circuit equals 1 rad/sec, or 0.159154 Hz, making a 10 to 90% rise/fall time of 2.12773 seconds. **Figure 1** scales the filter to a 100-psec rise time by multiplying all the capacitor and inductor values by the ratio $\tau/(2.12773)$, where τ is the desired rise time. This time-scaling operation leaves the resistor values unchanged.

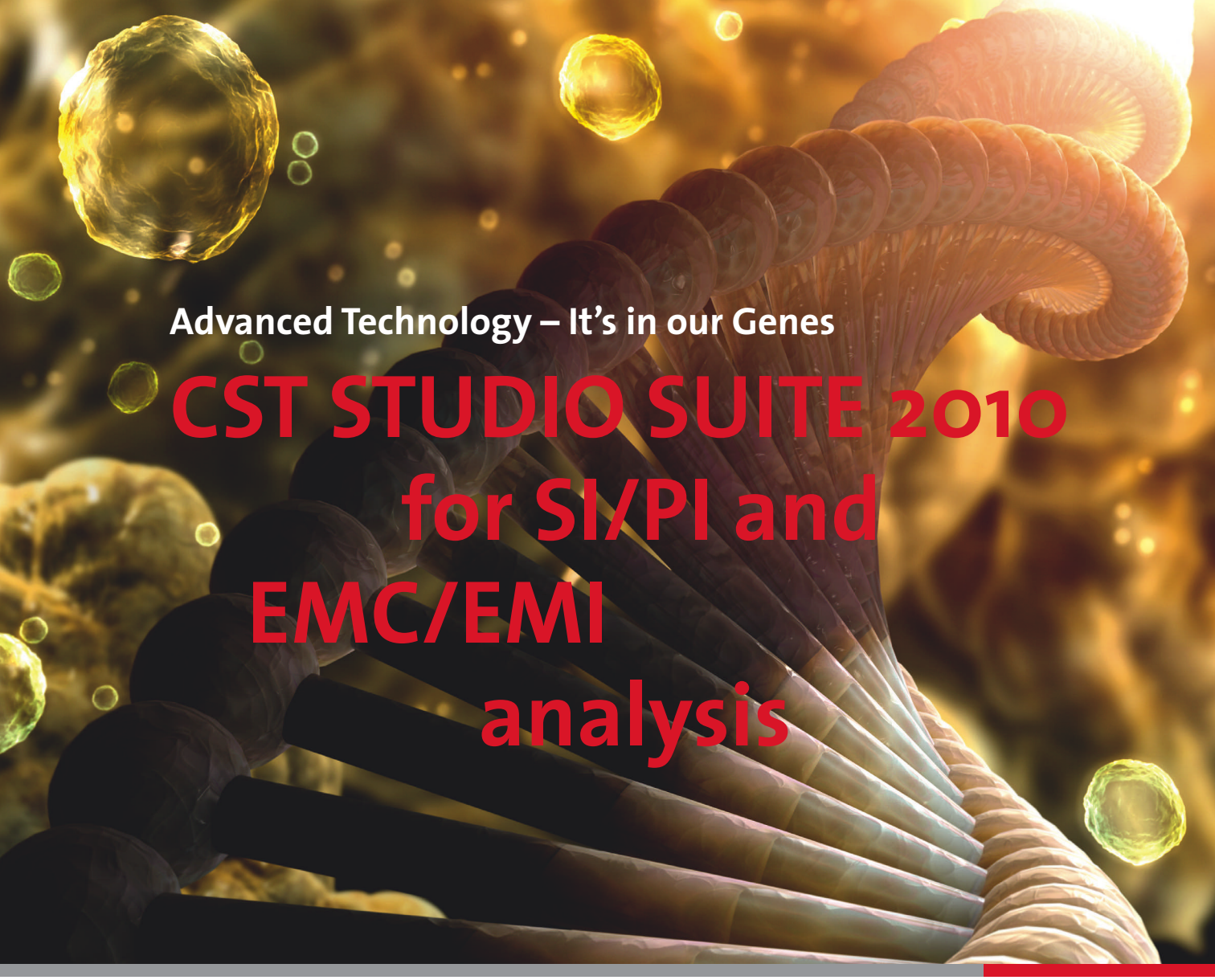
The combination of impedance- and time-scaling operations in **Figure 1** produces a 50Ω filter with a 100-psec rise and fall time. The filter tracks true Gaussian behavior down to −40 dB within ±1 dB, with a slope of 60 dB per octave after that (**Figure 2**, which is available in the Web version of this article at www.edn.com/091203hj). The nominal delay of the 10-pole model, from zero to 50%, is 1.485 times the 10 to 90% rise time. Remember this delay when making your timing calculations. You'll see it in the Spice model.

Always follow Zverev's filter with a buffer. In Spice terminology, a perfect buffer is a VCVS (voltage-controlled voltage source). The buffer prevents any attached loads from changing the filter's performance. Connect your driver's source-resistance and package models to the output of the buffer. EDN

REFERENCE

1 Zverev, Anatol I, *Handbook of Filter Synthesis*, John Wiley & Sons, New York, 1967.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.



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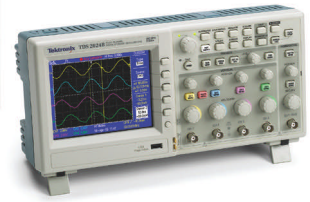

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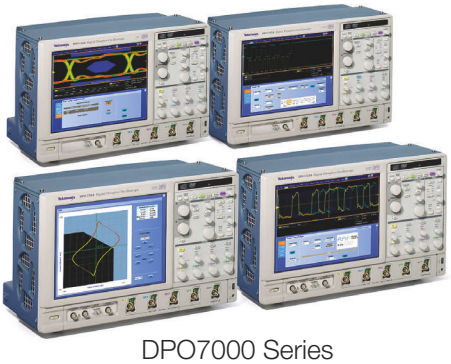

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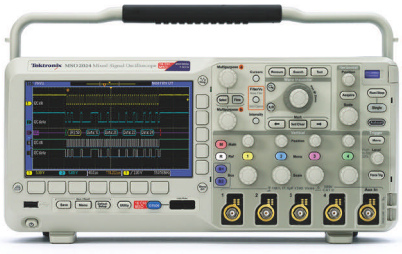

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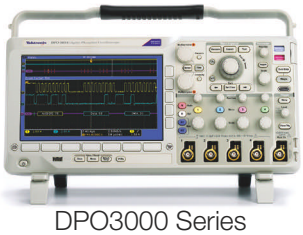

DPO3000 Series
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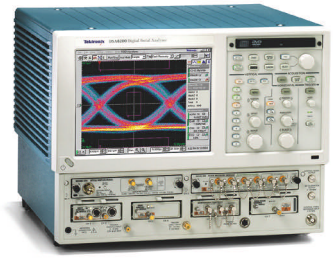

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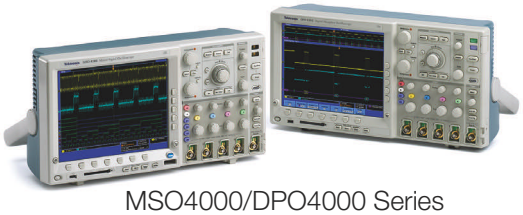

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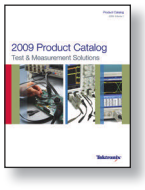

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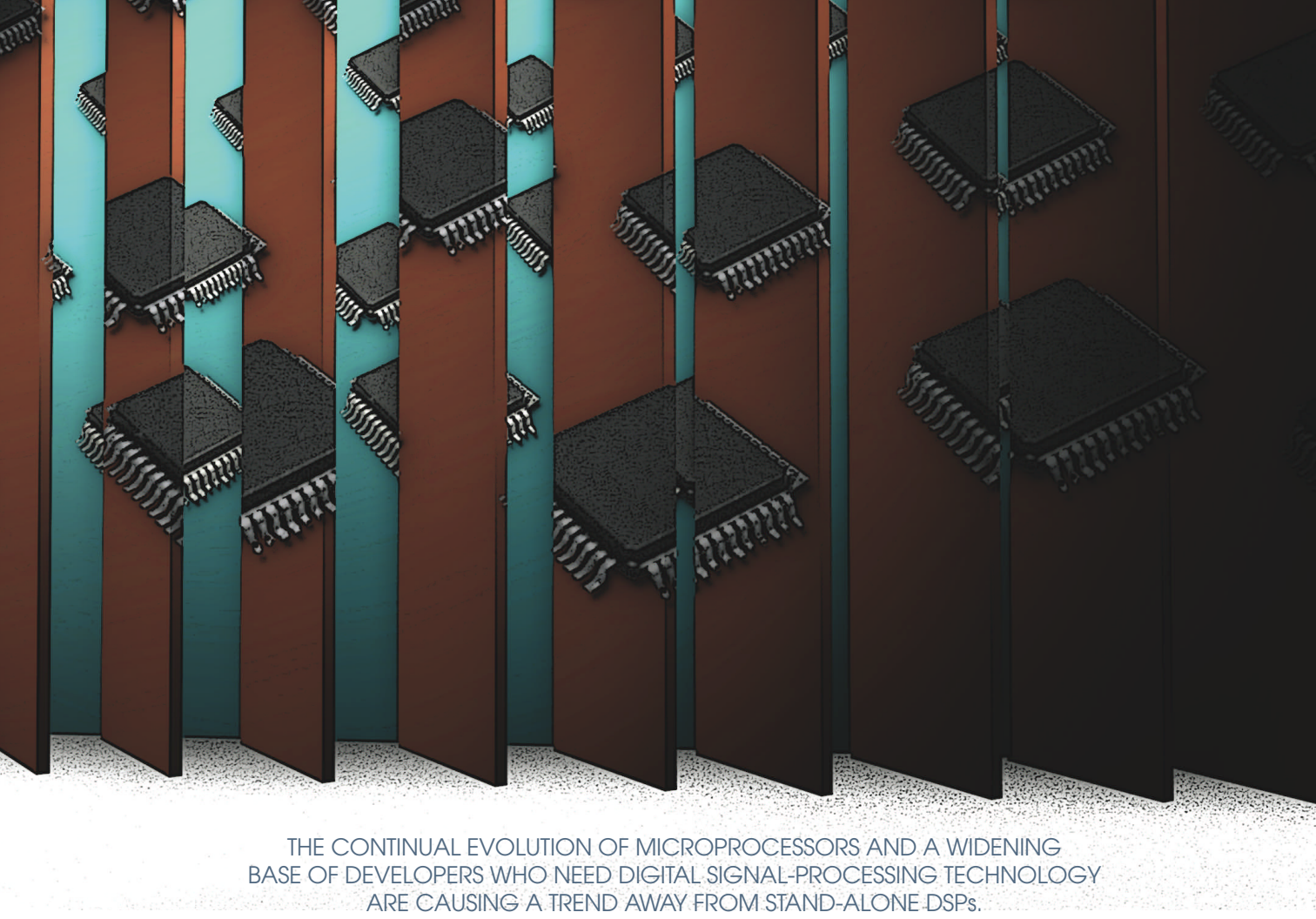

THE CONTINUAL EVOLUTION OF MICROPROCESSORS AND A WIDENING BASE OF DEVELOPERS WHO NEED DIGITAL SIGNAL-PROCESSING TECHNOLOGY ARE CAUSING A TREND AWAY FROM STAND-ALONE DSPs.

The evolving landscape of DIGITAL SIGNAL PROCESSING

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

Is the stand-alone DSP a dying breed? It may not exactly be dying, but the DSP is not front and center as it used to be. In 2006, *EDN* changed the name of its annual DSP Directory to the Digital Signal-Processing Directory (**Reference 1**). This subtle change recognizes that digital-processing options have commercially expanded beyond just software-programmable-processor devices and core offerings to include other options, such as programmable fabrics, IP (intellectual-property) blocks, and mixed-processing SOCs (systems on chips). These processing options complement as well as compete with each other because each faces a different set of constraints (**Reference 2**).

Signal processing involves mathematical manipulation for transforming—using filtering, Fourier transform, compression, decompression, synthesizing, recognizing, enhancing, encoding, decoding, and other methods—a set of data or a stream of signals. The continual advancement of microprocessors and growing base of developers who need this technology are leading the trend away from stand-alone DSPs.

The war between FPGAs (field-programmable gate arrays) and DSPs has died down over the past few years. Both camps have realized that they best serve different types of problems and that it is common for an FPGA and a processor to be operating side by side in one design. FPGAs can leverage arbitrarily wide signal-processing algorithms acting as hardware-acceleration blocks. This ability gives them an advantage over DSPs when the signal-processing algorithm is sufficiently wide enough that it can efficiently use more than the available processing units in the DSP. However, working with FPGAs is more complex in part because of their hardware-design flow. For example, Xilinx is focusing on making the FPGA easier to use, according to Tom Hill, senior mar-

keting manager for DSP solutions at the company. Xilinx accomplishes this task by abstracting the complexity of the design process, including accommodating a C-design flow and C-synthesis tools for hardware and software partitioning.

As microprocessors continue to benefit from Moore's Law, they can incorporate multipliers and specialized circuits, including specialized bus architectures and memory hierarchies, to improve their computational performance. Some of today's microprocessors deliver good computational performance, low cost, and high energy efficiency. If these parameters are good enough, these microprocessors let designers add and accommodate signal processing in a design—within a single chip. These processors do not necessarily deliver the best-in-class processing performance, cost, and energy efficiency, but they offer other system-level advantages, including bill-of-materials cost savings or a familiar design flow, and can thus be better choices than stand-alone DSPs.

WHAT'S IN A NAME?

As signal processing expands into more applications, ease of use becomes a critical concern despite the fact that designers historically often associate the term "DSP" with complexity. Early DSPs involved architectures that focused on extracting the maximum processing performance rather than on the ease of transforming mathematical algorithms into silicon and software implementations. As these processors evolved and were able to use more transistors with each new generation, they could better accommodate the transformation in various ways. Processors that allow programming in C, for example, help with this transformation.

Consider how Texas Instruments identifies its TMS320C2000 platform. The company once referred to these devices as DSPs with controller capabilities. A few years ago, however, these processors became known as DSCs (digital signal controllers). The company recently removed the C2000 from the 2009 *EDN* DSP Directory and now refers to it as a real-time microcontroller, even though the underlying architecture has not changed. The explicit focus has changed, however, to making the surrounding development-support environment more comfortable to microcontroller developers.

AT A GLANCE

- Embedded signal processing is quietly appearing within more processing options and application designs.
- Silicon providers are building application-targeted products to support the casual use of signal processing.
- Each skill for developing signal processing works at different levels of abstraction and with different natural data forms.

You may think that manufacturers taking this tack are being disingenuous, but keep in mind that many processor offerings place the focus on the target application and only imply the signal-processing capability. Examples include the Analog Devices Blackfin audio, video, and communications processors; ARM processors with Neon or accelerated multimedia IP; Freescale Power Architecture with Altivec extensions; Infineon TriCore automotive and industrial processors; Intel Pentiums with SSE (streaming single-instruction/multiple-data extensions); Microchip DSPic motor-control and power-conversion DSCs; NXP CoolFlux processors; Tensilica Xtensa audio and video engines; and Texas Instruments DaVinci and OMAP (open-multimedia-applications-platform) processors.

Each of these processors incorporates signal-processing architectural features from which their target application benefits. Application-specific algorithms or signal-processing libraries are available with many of these devices not only to improve time to market but also to enable developers to add capabilities to their designs without becoming experts about the new functions. Processor vendors are bundling silicon and software to simplify audio and video processing and other applications.

CASUAL-USER ADOPTION

Identifying processors by their target application reflects the trend for silicon providers to offer application-targeted products or implemented reference designs that comprise not only the hardware but also the appropriate software components that work with that hardware. Developers can buy or license targeted implementations for a growing array of signal-processing functions, such as compression, audio, and video encoding and decoding. These developers' focus is shifting from how to build core functions to whether an implementation meets performance, price, energy, time-to-market, and integration goals. Algorithm and system providers who can find the balance between delivering processing performance, energy efficiency, algorithm flexibility, and robust system integration should stand out in this increasingly competitive area.

The signal-processing nature of the bundled software in these offerings is sometimes less obvious. For example, touch sensing is such a popular capability that many processor vendors this year rolled out or updated touch-sensing support for their devices. These packages include processor targets with software and demonstration kits to ease the learning curve for developers trying to use the technology. The developer targets an API (application-programming interface), which hides from the developer much of the complexity of accessing the touch sensors. Managing and interpreting the touch-sensor inputs usually require significant amounts of signal processing, especially with the multitouch products, to filter and calibrate the sensor to deliver a consistent and reliable input source. Processor vendors are building their own in-house touch-sensing expertise and abstracting the complexity from the end developer. This step allows the developer to focus on higher-level interpretations of the touch inputs, such as recognizing command gestures.

This industrywide trend is moving digital signal processing to the level of a deeply embedded technology in which a growing percentage of developers are not concerned with the implementation details of "commodity" signal processing. This trend enables silicon providers to reach the larger set of developers who are not signal-processing experts without encumbering them with the learning curve of implementing these algorithms from scratch. It also makes irrelevant the dirty secret of the most optimized signal-processing implementations—that the software is often hand-optimized assembly or C code with heavy usage of compiler intrinsics to squeeze the best performance from the underlying hardware. Developers can continue to use the familiar C-code design flow for their value-added part of the system without

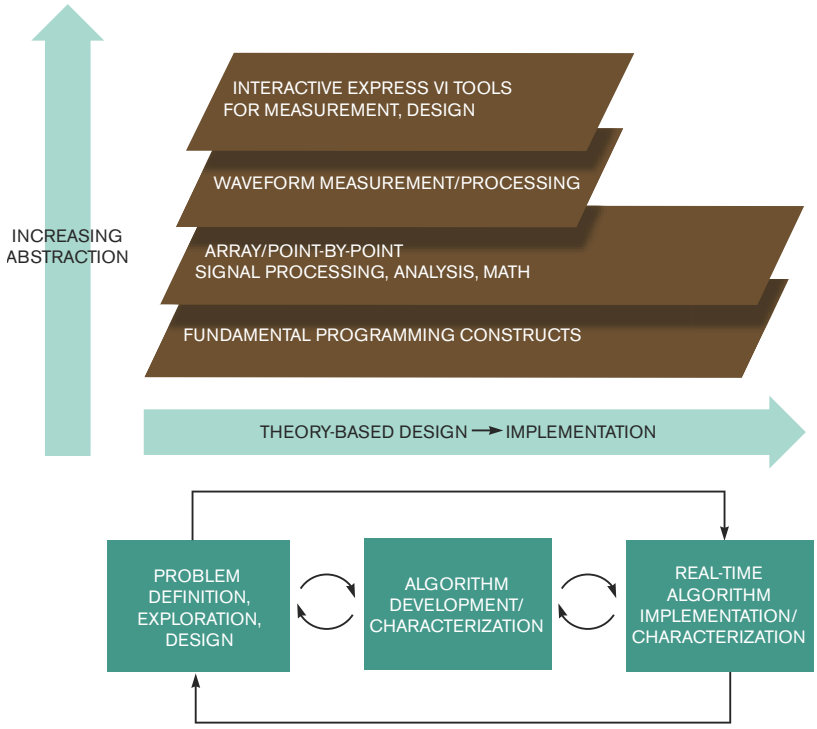

Figure 1 The stacked blocks represent categories of functions, based on the level of abstraction of their programming interface and number of encapsulated functions (courtesy National Instruments).

concern for implementing the coding of the licensed, timing-critical "heavy lifting." It also provides the groundwork for certifying the algorithmic implementations as the silicon providers continue to build their core group expertise.

This emerging abstraction layer helps support the exploding increase in the number of casual users who are adopting signal processing. However, it represents another layer of complexity for the silicon providers' development support because the power and intermediate users of these processors still need visibility down to the metal to support their innovation explorations. Piergiovanni Bazzana, an application developer at Atmel, describes two of the company's customers that wanted to employ the same Atmel dual-core microcontroller/DSP processor for the same type of end product. The smaller company wanted to use a single graphical programming tool to develop both the microcontroller and DSP cores because the company had fewer resources to dedicate to the project and was interested in implementing compliant standard algorithms. The

larger company wanted separate development tools for each target processor because it not only had more development resources but also planned to incorporate some innovations into its algorithm implementation that required the company's designers to be able to see deeply into the target system.

Designs that target standard signal-processing algorithms are appropriate for a library approach. The developer needs to read and understand the standard documentation or reference code to understand compliance issues; the effort then becomes a way for designers to optimize their designs to the target architecture. For a given processing option, the silicon provider can amortize its expertise with the signal-processing function and its architecture as a package across several customers. In contrast, designers who are implementing algorithmic innovations must optimize not just the implementation to the target but also the physical phenomena to provide insight in refining the algorithm. In this case, a C-based approach, with compiler intrinsics if necessary, is more appropriate because it provides the flexibility that a library approach cannot.

For related blog posts about embedded processing, go to www.edn.com/blog/1890000189.html.

For a related article about processing options, go to www.edn.com/article/CA6662624.

For related material about digital signal processing, visit www.edn.com/dspdirectory.

For a list of Web sites for the companies this article mentions, go to www.edn.com/091203df.

NECESSARY SKILLS

Building a signal-processing system requires exploring and refining the algorithm, implementing the algorithm on a target, and specifying and verifying the system-level timing. These skills can reside within a single person or a team. According to Ken Karnofsky, senior strategist for signal-processing applications at The MathWorks, communication among people with any of these skills involves a translation challenge because they each have different natural work products, data, and work flow. Algorithm exploration is math-intensive and requires an understanding of the physical phenomenon that you are modeling. Implementing the algorithm on a target processor does not require the same level of understanding of the mathematics or the physical phenomena. Rather, the developer's expertise focuses on how to organize and schedule the processing resources to provide robust delivery of good-enough performance and energy efficiency. Verifying the system-level timing requires identifying the various operating conditions that the end system must support for robust operation.

Tools such as The MathWorks' Matlab and Simulink and National Instruments' LabView development tools help algorithm developers with the exploration of algorithms with varying levels of abstraction and high-level mathematics simulation (**Figure 1**). Working at a high abstraction level is generally useful when

defining problems and exploring design possibilities. In the LabView example, Express VIs (virtual instruments) present an interactive, configuration-based user interface to, for instance, synthesize test signals, see the result of applying a window, or examine a spectrum. Less abstract tools, such as those from the array/point-by-point library, are more flexible and programmable to enable custom algorithm development and implementation.

These tools are also helping to bridge some of the transitional challenges between algorithm development and implementation by supporting autogenerated code that executes on a target processing board. For low-volume or high-margin applications, the autogenerated code may be sufficient for rapid prototyping or fast time-to-market exploration. Using the autogenerated code on a target board can provide the algorithm developer a more direct understanding of the challenges facing the implementation developer.

Implementing and optimizing the algorithm on the target architecture involves using the development tools the silicon provider supports for the target system. The autogenerated code can assist in comparing the trade-offs among target architectures with the increasing use of compilation-time replacement technology that allows target substitutions to take place. For those algorithms that require special resources to attain their processing-performance constraints, the developer may have to use compiler intrinsics or hand-optimized assembly. Standard ANSI C code does not provide compilers with visibility into dynamic memory usage, so the compiler must make a number of assumptions to generate good code. Compilers are strong on scheduling register and internal-memory accesses because they have direct management over those resources, but they are weak on scheduling DMA (direct memory access) because they do not have complete control over the resources they are accessing. Compiler intrinsics allow the developer to more directly specify assumptions and resource allocations.

System-level timing skills become more important as the system performs more tasks with shared resources. Early DSPs focused on low-overhead looping at the expense of interrupt support. Contemporary processors support many interrupt sources, especially for connectivity capabilities. Signal-processing algorithms are increasing in complexity, including performing processing on a data-point-by-data-point basis, potentially complicating system-timing analysis. Manufacturers are increasingly commoditizing successful signal-processing algorithms and embedding them—whether as bundled software with a silicon target or as licensable software implementations—in the processing components of embedded designs. As this situation evolves, developers will spend more time specifying and verifying the system-level performance and then developing and implementing the algorithms.

The quality of a system depends on the guarantee of the algorithm's real-time system-level maximum load or worst-case latency. The highest-quality system bases the design on the worst-case path or latency impact and meets the real-time threshold under all cases. A moderate-quality system defines a threshold in which it is acceptable to experience some error and miss the real-time threshold but still recover; the system is robust enough to handle discontinuities.

Gene Frantz, principal technical fellow at Texas Instruments, observes that many DSP users are more inexperienced than their predecessors. This fact should influence how universities teach signal processing. As more signal-processing algorithms become subject to commodity implementations, most designers will find more value in focusing on how to combine the building blocks in innovative ways rather than building all of the blocks from the ground up. **EDN**

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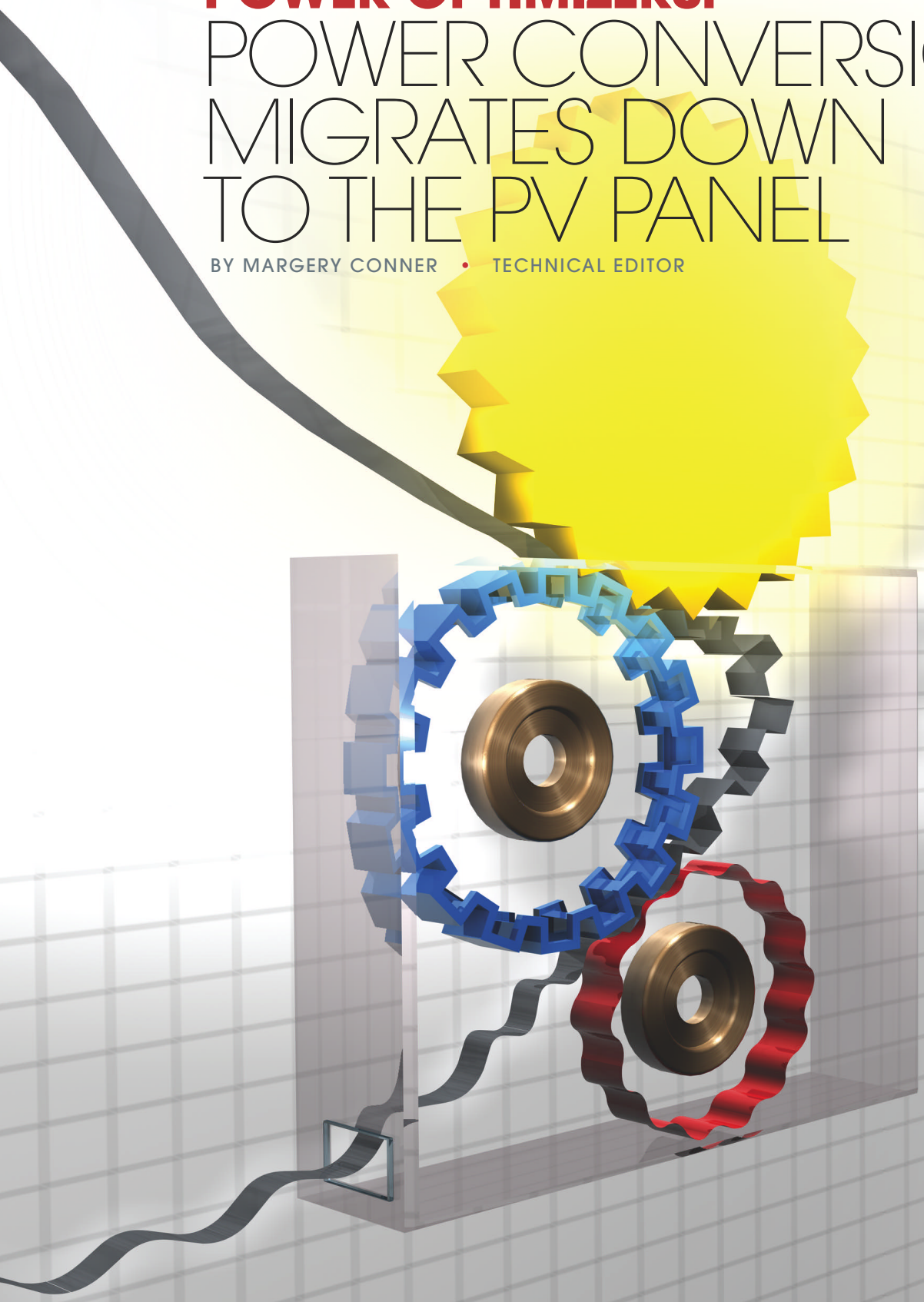
MICROINVERTERS AND POWER OPTIMIZERS: POWER CONVERSION MIGRATES DOWN TO THE PV PANEL

BY MARGERY CONNER • TECHNICAL EDITOR



ALTERNATIVE FORMS OF POWER HAVE BECOME INCREASINGLY POPULAR AS UTILITIES REACT TO RISING FUEL PRICES AND GOVERNMENT MANDATES. PHOTOVOLTAIC CELLS USUALLY RECEIVE MOST OF THE ATTENTION AS SOLAR-ENERGY COST DRIVERS, BUT THE AC/DC INVERTER DESIGN IS EQUALLY IMPORTANT TO OVERALL SYSTEM EFFICIENCY AND COST.

The size of solar-power installations is shifting away from the multimegawatt solar farms of 10 to 20 years ago toward smaller installations of 1 MW or less. Factors driving this trend include utilities' increasing use of residential and industrial rooftops as localized solar-power-generating stations, thus reducing the need for conventional power plants, and the emergence of solar-PPA (power-purchase-agreement) companies, which install rooftop solar panels on homes and small businesses in exchange for access to the generated power (**Reference 1**).

Small installations differ in some ways from massive solar farms. For example, solar-farm panels all face in the same direction and generally experience the same amount of sunlight. They typically encounter no obstacles, such as trees or utility poles, which can obstruct the sun on different panels at various times of day, causing panel-to-panel variations in power output. Small solar installations, in contrast, must accommodate a variety of roof lines, especially in residential installations, which lack uniform panel orientation and thus can yield suboptimal power generation.

Small installations do share some features in common with solar farms, however. They both require regular cleaning, for instance, and all panels age at slightly different rates, causing a variation in panel outputs. Both small and large solar-power installations also use PV (photovoltaic) solar panels, which comprise arrays of solar cells and typically have a voltage output of 25 to 30V dc. Users of these panels usually cascade them in series, forming strings with a typical output of approximately 300 to 350V dc. They can also further parallel these strings for large solar arrays. The output of these arrays feeds into a central inverter that transforms the dc voltage to ac and synchronizes the ac voltage to the grid. The power output of inverters for large arrays of solar panels can range to 6 kW and beyond; central residential inverters range from 2.5 to 3 kW.

However, not all solar panels are created equal, and inconsistencies in manufacturing, obstructing elements, dirt, aging, and other factors can cause panels to produce different amounts of power. Each panel has an optimal power point, which affects the optimal power point for the string and, ultimately, the array. If the installation draws too much power from the array, the output power drops. If it draws less power, the installation cannot make efficient use of the array.

Algorithms can find the power "sweet spot," which ideally would occur at each panel. In a common technique, "disturb and observe," the power-transformation circuitry attempts to draw a little more current to see whether the voltage drops. The algorithm performs MPPT (maximum-power-point tracking), during which it searches for the point at which it gets the maximum power from a module. In traditional solar installations, this process takes place at the central inverter. With a central inverter, you most likely will find a local maximum rather than an absolute maximum for the array because the performance of one poorly performing panel will dominate the algorithm. If all the panels are well-matched, the difference between the true maximum and the local maximum power points will be insignificant. You can't count on having well-matched panels, though, because of aging differences, a passing cloud cover, or the presence of dirt. One poorly performing module dictates the power that the other modules in series with it deliver.

One approach to this problem is to use a dedicated microinverter for each panel that finds the maximum power

point for each panel rather than use one inverter to find the maximum for all the modules. The output of the dedicated microinverter goes directly to the grid or ac power-distribution circuit. European solar companies tried this approach more than 10 years ago using ac panels, each of which produced an ac voltage and tied into the grid. The approach has economic drawbacks, however, because it costs more to use one inverter—albeit a small one—per panel than it does to use just one central inverter or even one inverter on each string of the array.

Large installations minimize panel variations with regular cleaning schedules and by avoiding or removing shading obstacles. However, with the trend toward smaller installations, architectural limitations may dictate varying panel orientations, and utility poles and trees can cause individual panels to become dirty or be in the shade at different degrees and at various times, so you would need to optimize each panel.

INSTALLATION COSTS

Central inverters are also large and heavy, requiring the installation of cement pads and centralized connections to the grid, increasing installation and labor costs. A 200W microinverter that must handle only 30V-dc input becomes attractive for small installations, including users wanting do-it-yourself setups. In addition, a microinverter's module output power is only 200 to 300V ac. In contrast, a panel array's output to a central inverter can be as much as 600V dc in the United States and 1000V dc in Europe—hazardous levels for installers, maintenance personnel, and emergency responders.

AT A GLANCE

- The move toward smaller installations has made solar radiation less uniform for each PV (photovoltaic) panel.
- Microinverters and panel power optimizers can be cost-competitive with large central inverters when you figure in labor and installation costs.
- Reliability over the 20-year lifetime for power installations is a challenge for electronics.

Enphase Energy, among the first companies to deliver microinverters, sells a 200W device for approximately $200, or about $1/W, compared with a 3-kW string inverter, which sells for approximately $2000, or about 67 cents/W. Enphase suggests that its products' lower installation and investment costs compensate for the additional 33 cents/W.

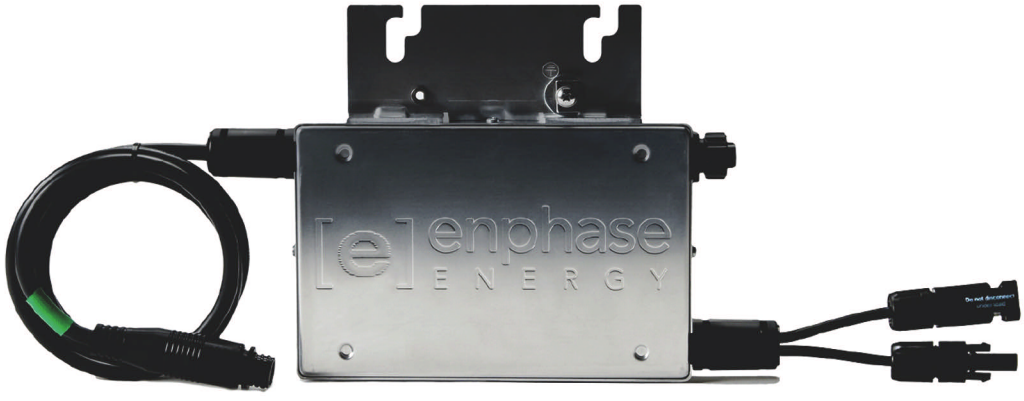
However, microinverters' reliability is just as big of a question as their cost. Common inverter topologies use electrolytic capacitors on their output filters. These topologies have a poor reputation for reliability, especially when you subject them to the elevated operating temperatures of solar installations. The likelihood of a failure due to an electrolytic capacitor increases when you go from using one central inverter to using 10 to 20 microinverters. Most solar panels have a guaranteed life of 25 to 30 years, and operators want a similar lifetime from their inverter circuits.

Enphase's Web site includes several white papers dealing with capacitors' reliability and lifetimes. One paper explains how the company uses more reliable electrolytics in capacitors than those that power supplies normally use (**Reference 2**). According to the company, higher reliability translates to a longer life in the real-world temperatures you find in solar installations. For traditional power converters, an acceptable useful life for capacitors operating in 85°C environments is as low as 2000 hours. Enphase microinverters use Nichicon capacitors that operate for 4000 to 10,000 hours at 105°C.

Capacitor lifetime is sensitive to temperature and follows the Arrhenius equation, which states that useful life doubles for every 10°C temperature drop. The NREL (National Renewable Energy Laboratory) solar-radiation database for the California desert town of Palm Springs in the summer lists a maximum ambient temperature of 46°C, resulting in a core temperature for the capacitor of 65°C, or 40°C lower than the 10,000-hour rating at 105°C, yielding a 160,000-hour operating life at this temperature (**Reference 3**). Enphase claims to have designed its microinverters "for a service life of 20 years," but the Web site guarantees its products for only 15 years.

INVERTER RELIABILITY

Enphase sells its stand-alone microinverters separately from the panels. The inverters can work with a range of solar panels, require no central inverter, and have almost 95% efficiency—compared with central inverters' 98% efficiency figure. They perform MPPT at the pan-



Enphase's 200W dc/ac microinverter optimizes the power at each solar panel and eliminates the need for a central inverter. Despite its reliance on electrolytic capacitors, the unit offers a 15-year warranty.

el, increasing the efficiency of each module.

However, according to Kevin Kayser, marketing manager for National Semiconductor's Phoenix design center, electrolytic capacitors aren't solely responsible for failure mechanisms in solar installations. "Talk to any system integrator out there, and they'll tell you the most unreliable component is the inverter," he says. "[The microinverter topology] multiplies the inverter throughout the array." The company's Solar Magic modules exemplify another panel-based power-management scheme that works with—rather than replaces—a central inverter. National Semiconductor coined the term "power optimizers" for dc/dc converters that optimize the power at each solar panel, adjusting current and voltage so that each panel outputs its maximum dc power. Solar Magic panel installations use a string topology and require a central inverter that performs MPPT. Each panel outputs maximum power, optimizing the string's performance. If one of the panel's voltage drops due to, say, the presence of dirt, Solar Magic algorithms adjust the module's current to arrive at the optimal power output.

"[Solar Magic's] dc/dc-conversion approach is less complex," says Kayser. "Microinverters boost a 28V panel to 350V dc and convert it to ac, touching the grid at every module. Because of the 60-Hz frequency of the grid, the capacitor must handle that frequency, requiring less-reliable electrolytic or film capacitors. [Solar Magic's] dc/dc approach uses ceramic capacitors."

National Semiconductor is not the only company in this market. SolarEdge has announced a similar dc/dc power-management approach at the panel level, but its technology requires a proprietary central inverter. The company embeds the panel-control electronics in the panel, rather than selling them as separate modules, and performs MPPT for each panel. SolarEdge then cascades the panels in strings with a fixed voltage output for each string and feeds them into a central inverter, which performs only dc-to-ac conversion because MPPT has already taken place at the panel level.

National Semiconductor's Solar Magic dc/dc converter optimizes power for each solar panel by adjusting the panel current if the panel voltage decreases. The panels cascade in series to feed into a central inverter that performs MPPT. End customers can expect to spend about $175 for each power optimizer.

For designers who choose to develop their own integrated panel converters, STMicroelectronics offers the SPV1020 PWM (pulse-width-modulation)-mode dc/dc boost-converter IC, which can maximize the power that PV panels generate independently of panel temperature or the amount of incident sunlight. The converter implements hardware algorithms to calculate the MPPT for PV cells within the solar panel. Because individual solar cells can begin to fail and disrupt the total panel's power output, panels typically have bypass diodes that switch poorly performing cells out of the internal PV-panel array of cells. The SPV1020 resides in the connection box of a panel and replaces the bypass diodes. The chip also integrates power MOSFETs that perform dc/dc switching and synchronous rectification. Like Solar Magic's technology, because the dc/dc conversion occurs at a relatively low voltage, the power converter can use ceramic capacitors rather than less reliable electrolytic capacitors.

Microinverter companies are focusing on squeezing every last bit of efficiency from their topologies, in part because of the need to deliver as much power as possible to their installation's customers and in part because they are competing with the high conversion efficiency of central inverters. The technology benefits from the increased efficiency of low-voltage switching elements. The voltage output of a solar panel ranges from 25 to 30V, so the first regulation stage in a microinverter typically uses 40V. These MOSFETs have over the last 10 years improved their on-state resistance by an order of magnitude. For example, Infineon's 40V Optimos-3 series has an on-resistance as low as 1.1 mΩ; 10 years ago, it was more than 10 mΩ. In addition, low-voltage MOSFETs' use in high-volume consumer products, such as on-board power regulation for desktop and laptop motherboards, has decreased their price. Microinverters also use high-voltage FETs for the final output-voltage phase-matching stage, which requires 600 or 800V MOSFETs. Infineon's CoolMOS technology has been on the market for more than 10 years and has during that time reduced the on-resistance to 20% or less. **EDN**

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BY HARLEY BURGER • LSI CORP

Preamplifier and read-channel design addresses hard-drive goals

THE HARD-DISK-DRIVE INDUSTRY IS FACING DIFFICULT CHALLENGES FOR INCREASING STORAGE CAPACITY AND ADDRESSING COST, PERFORMANCE, POWER-CONSUMPTION, AND OTHER IMPORTANT PARAMETERS. JOINTLY DESIGNING THE MEDIA, HEAD, FLEX, PREAMPLIFIER, AND READ CHANNEL PROVIDES A GOOD APPROACH TODAY AND LAYS THE FOUNDATION FOR FUTURE HARD-DRIVE GENERATIONS.

As the capacity of hard-disk drives continues to increase, the burden on the system to reliably access data on the media also increases. For read accesses in particular, this challenge is creating the need for ever-more-complex signal-conditioning and -processing algorithms to recover the data from the ever-decreasing signal quality—that is, lower SNR (signal-to-noise ratio)—of information coming off the media. To make the situation even more challenging, price, power consumption, and speed trends are all moving in difficult-to-address directions. Cost and energy draw must continue to decrease, and the rate at which the data comes off the disk must increase from one generation to the next. All of these factors make for a difficult but rewarding design challenge.

TECHNOLOGY OVERVIEW

Before delving into the benefits of jointly designing the preamplifiers and read channels, you should briefly consider the functions of each block. The preamplifier resides between the read head, which senses the bits on the disk, and the read channel (**Figure 1**). A primary function of the preamplifier is to faithfully transmit the noisy signal from the head to the read channel with minimal distortion and other degradations. The preamplifier accomplishes this objective by first amplifying the head signal and then driving it to the read channel (**Figure 2**).

The first function of the read channel is to further condition the partially processed signal from the preamplifier through a series of filters and gain stages (**Figure 3**). From there, the conditioned signal goes to the signal-processing section for conversion into a faithful representation of the original digital data that was previously written on the disk.

The signal-processing section typically comprises a detector, an inner code, and an outer code (**Figure 4**). The signal-processing function block implements complex algorithms that have evolved over time from a simple peak-detection system to a full-blown LDPC (low-density-parity-check) system in migrating toward the Shannon capacity limit (**Figure 5**).

SYSTEM OPTIMIZATION

To achieve an optimal result, engineers must model, simulate, and design the datapath from the head to the output of the read channel as a system, not simply as a series of independent blocks. A system-design approach allows you to make the proper trade-offs with respect to performance, power, and cost. The signal coming from the media must travel though a complicated path before it becomes valid data at the output of the read channel. It flows through the head, down a flexible transmission wire, into the preamplifier for boosting and filtering, down another flexible transmission wire, and then into the read channel's signal-conditioning block, where it is further amplified, filtered, and linearized.

Each of these interfaces requires proper design to ensure optimization of the signal bandwidth, dynamic range, termination impedances, and transmission effects. Failure to fine-tune

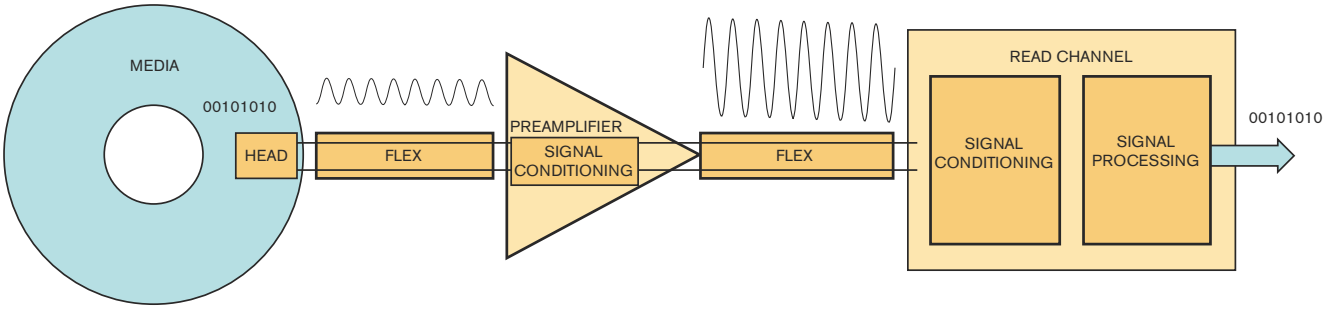


Figure 1 The hard-disk drive's read-signal path is complex and full of opportunities for optimization.

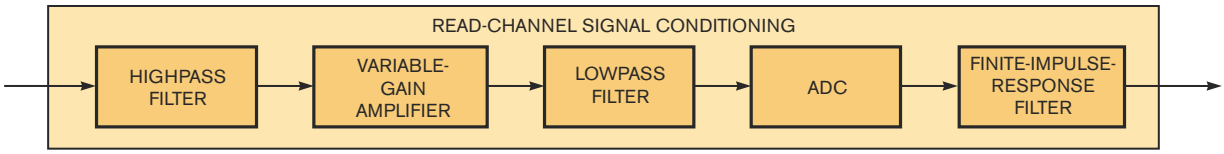


Figure 2 Read-channel signal conditioning encompasses several steps.

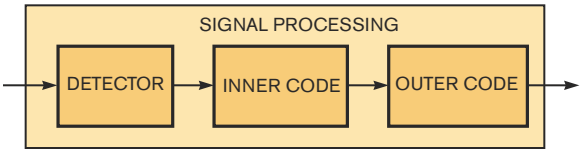


Figure 3 The overall signal-processing function subdivides into three stages.

the signal-conditioning path will lead to suboptimal performance for which the read channel's signal-processing block may be unable to compensate.

Because both the preamplifier and the read channel bear the signal-conditioning burden, the trade-offs you make in these areas can both optimize performance and lower the overall system power consumption and cost. Manufacturers typically build the read channel in a fine-line CMOS process for large digital circuits that use low-voltage power supplies. Therefore, you decrease power consumption and cost in the silicon area when you minimize the number of pure analog circuits you use in favor of digital signal conditioning and digitally assisted analog circuits. These circuits can then run on the core transistor's power supply—typically at 1V—instead of the I/O's power supply, which is typically 2.5V.

Digitally assisted analog circuits can, for example, comprise DACs to set up the gain in a variable-gain amplifier (**Figure 6**). They can also find use in setting the pole frequency in a lowpass filter instead of relying on the traditional variable-resistor analog-feedback technique. Small, low-power DACs can also zero out offsets, allowing the use of high-speed and low-power core transistors.

Manufacturers usually build preamplifiers in an older, less-expensive bipolar or Bi-CMOS process for analog performance using higher-voltage power supplies. Pure analog amplifiers and filters are therefore efficient; digital signal-conditioning circuits, however, are not. The logic in a preamplifier process is typically lower-performing and runs from a higher-power supply. Therefore, it is critical to properly divide the signal-conditioning task between the preamplifier and the read channel.

Another benefit of designing the preamplifier and read channel together is that you can save power by taking advantage of your knowledge of mode transitions that pass between the blocks. This premonition allows for the activation or shutdown of function blocks at precise times to ensure that circuits power up only when absolutely necessary. With previous implementations, function blocks would remain in a high-power state because they would not know when the next command was coming. They could not enter into a low-power state because the transition back to fully on mode would take too long to settle out. However, advance knowledge means that it is no longer necessary for circuitry to perpetually remain in a high-power state. It can power down and then later move back to fully on mode through an early wake-up signal. The end result is a system with a lower power draw, an important feature for hard-disk drives.

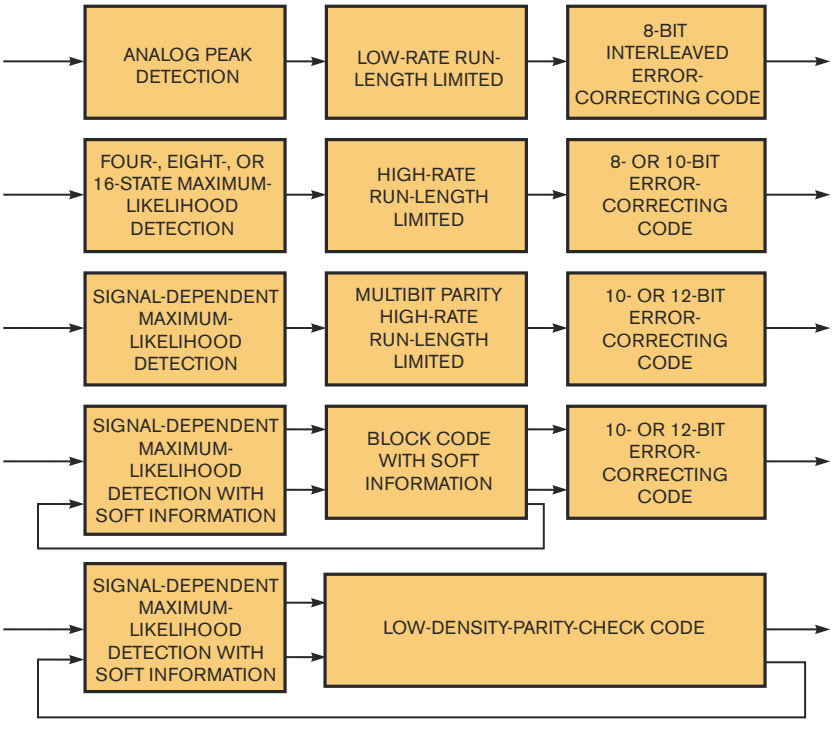


Figure 4 Signal-processing algorithms have grown steadily more complex over time.

You can achieve further system-performance improvements by minimizing the distance between the head and the data on the media (**Figure 7**). The lower the head flies over the media, the stronger the signal becomes, thereby improving the SNR. Therefore, a control loop at a good flying height between the head, the preamplifier, and the read channel is critically important. You must provide compensation within the signal-processing block for the nonidealities of signal-conditioning circuits to control the flying height of the head.

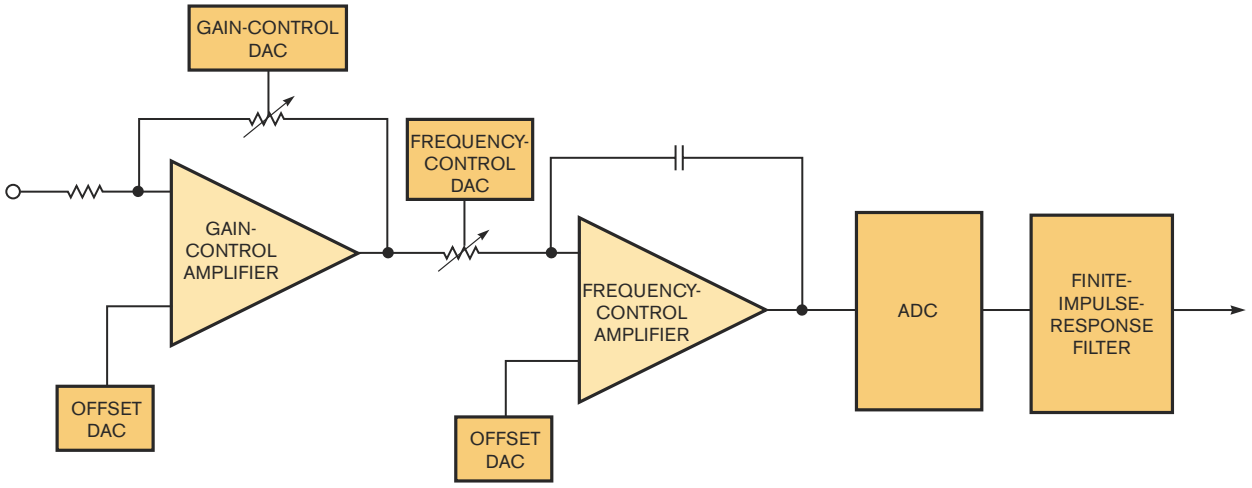


Figure 5 Digitally assisted circuits, such as DACs, are optimal for the pure CMOS processes manufacturers typically use to fabricate read-channel ICs.

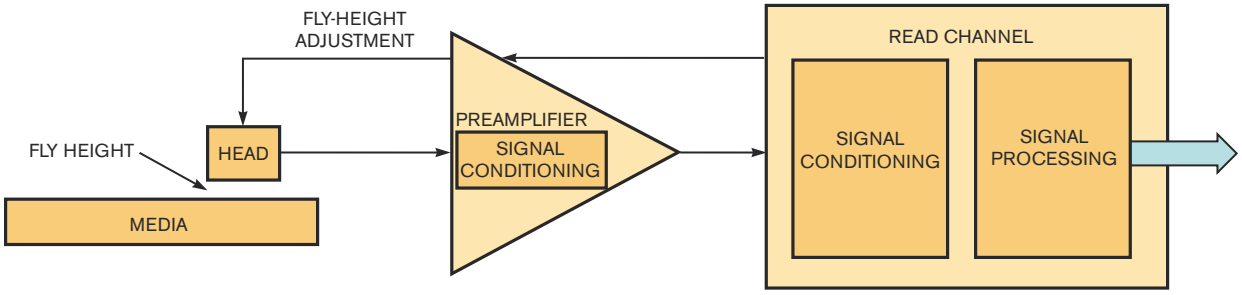


Figure 6 The closer the head is to the media, the better the SNR is, but the overall design is more difficult.

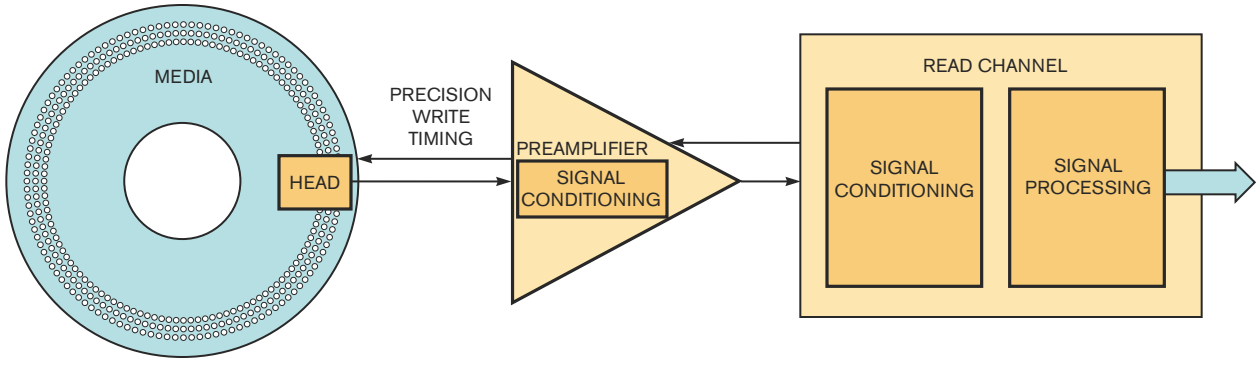


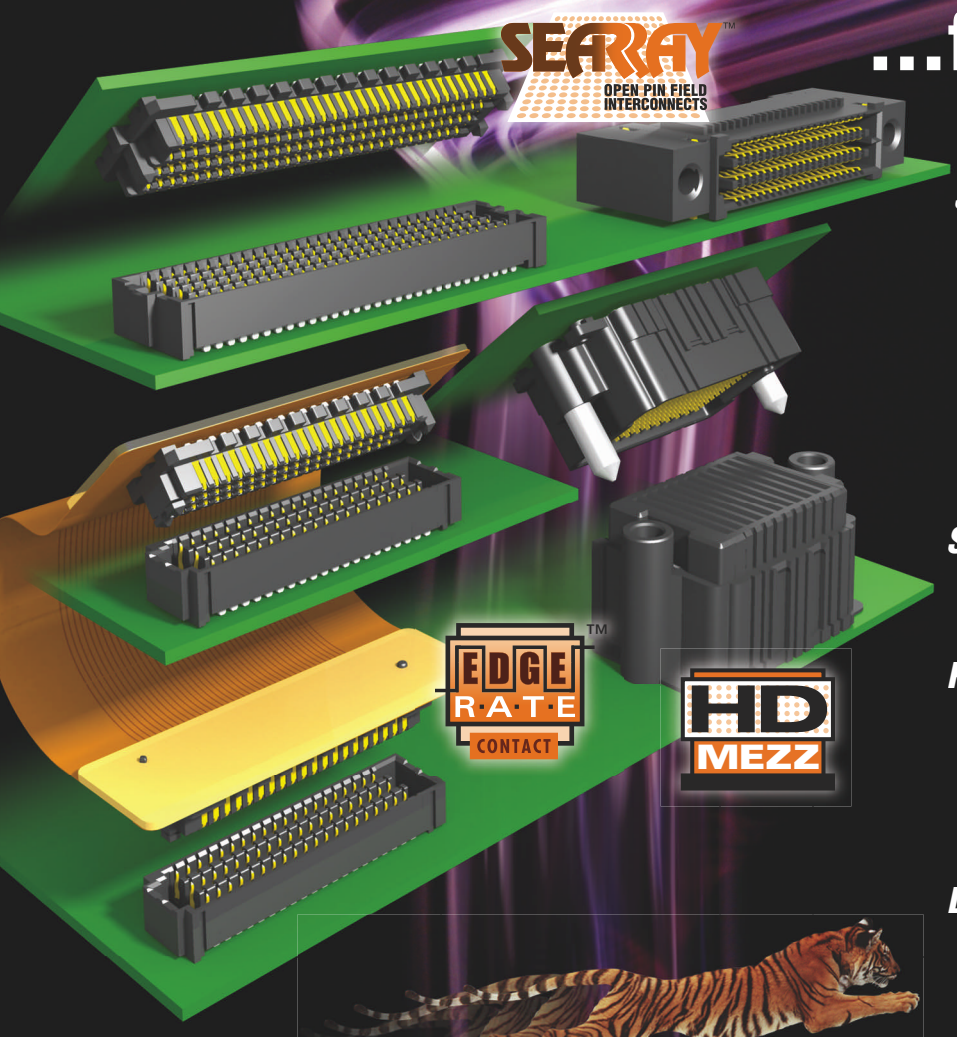
Figure 7 A pending transition from homogenous magnetic media to the patterned successor will create additional challenges and opportunities.

In the near future, the media will evolve from a continuous magnetic plane into patterned media in which each bit is physically isolated from others. This transition will greatly complicate the writing of the data to the media because it will require precise control of the time that the data writes to the bit cell. You must comprehend and compensate for delay variations with respect to environment, voltage, and process. You can accomplish this objective only by using a well-controlled feedback loop, in which you design the preamplifier and the read channel. EDN

AUTHOR'S BIOGRAPHY

Harley Burger is a fellow at LSI Corp, with a focus on designing and marketing approaches for hard-disk drives. With more than 20 years of industry experience, he leads the exploration of technologies in media, head, and signal-processing areas aimed at increasing hard-disk-drive capacity. Burger's career began at AT&T Bell Laboratories, and he remained there after the evolution of the company through its subsequent years as Lucent Technologies and then Agere Systems, which LSI acquired. He currently holds two patents.

The path of least resistance



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Taming inaccurate real-time clocks

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In modern multimedia systems, maintaining an RTC (real-time clock) is an important task. An RTC supports displaying the play time on a media player and the call details in a video phone. One way to provide the RTC feature is to use an RTC chip. An RTC chip uses an internal crystal oscillator as a reference and keeps track of time. Most RTC chips maintain time in seconds, minutes, hours, days, and years, and they also account for leap years. You can read the current time from certain registers in the RTC chip using an SPI (serial-peripheral interface) or a two-wire I²C (inter-integrated-circuit) interface. Some systems use an auxiliary microcontroller to perform user-interface and other housekeeping functions, and it makes good design sense to have the RTC function on this microcontroller. In this case, the microcontroller maintains a count of elapsed seconds using an external crystal as a reference. The conversion of this counter to seconds, minutes, hours, days, and years takes place in software.

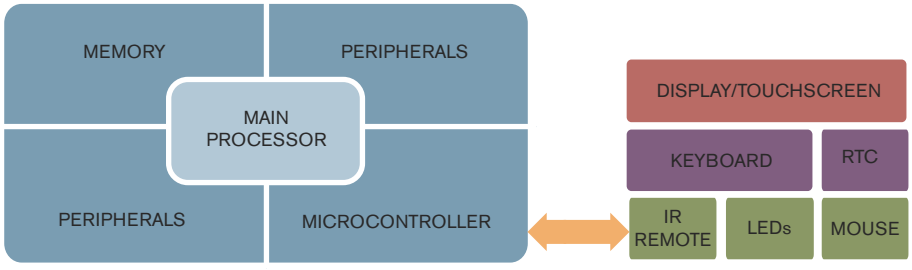

Figure 1 Using a microcontroller to implement an embedded RTC along with user interfaces and other housekeeping functions results in a single-chip implementation for multiple functions and results in a lower design cost.

A dedicated RTC chip eliminates the onus on software when using an embedded-RTC implementation. Also, the crystals in many chips are temperature-controlled and provide accuracies of 2 to 3 ppm (parts per million). On the other hand, using a microcontroller to implement an embedded RTC along with user interfaces and other housekeeping functions results in a single-chip implementation for multiple functions and results in a lower design cost (**Figure 1**).

However, the accuracy of the time the microcontroller maintains depends heavily on the accuracy of the crystal it uses as a reference. Typical crystals have accuracies of 20 to 45 ppm. This range translates to an unacceptable error of 1.7 to 3.9 seconds/day. One obvious way to alleviate this problem is to use a highly accurate crystal, but this approach translates to an increased design cost and hence is not viable for cost-sensitive embedded designs. Another approach uses a calibration algorithm that can implement an accurate embedded RTC in the presence of an inaccurate crystal in the system. Some embedded-RTC algorithms use a look-up table to compensate for the crystal inaccuracies. A generic approach is adopted here that adjusts the calibration factor in tune with changes in crystal, system, or temperature and aging.

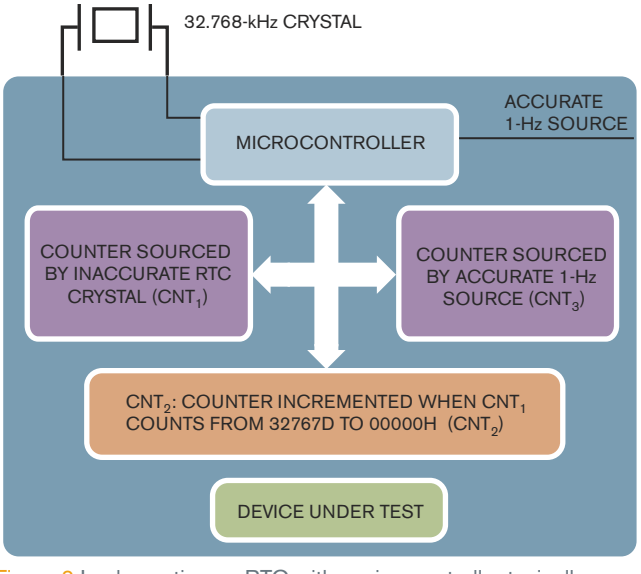

Figure 2 Implementing an RTC with a microcontroller typically uses the signal from a 32.768-kHz crystal oscillator, which increments a counter, such as the 16-bit CNT_1 counter.

CALIBRATION

Implementing an RTC with a microcontroller typically uses the signal from a 32.768-kHz crystal oscillator, which increments a counter, such as the 16-bit CNT_1 counter (**Figure 2**). The duration of 32,768 clock cycles corresponds to an interval of 1 second. For each second, when the system is on, CNT_1 increments from 00000d to 32767d. Because the crystal is inaccurate, CNT_1 overflows from

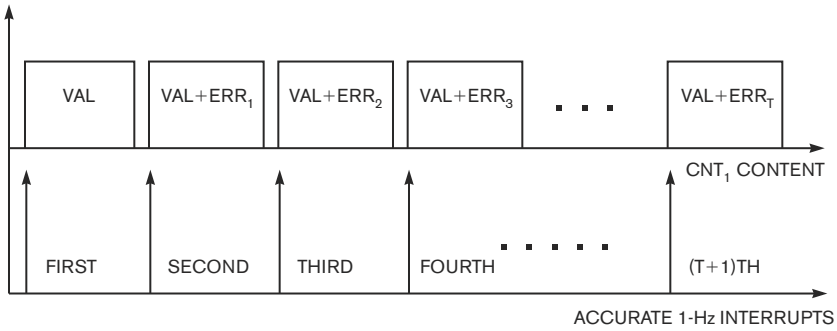

Figure 3 The value in CNT_1 on the first 1-Hz interrupt is VAL. If the RTC crystal is accurate, the value in CNT_1 at any of the 1-Hz interrupts would be VAL because CNT_1 would have overflowed and counted up to the same value each second. However, this scenario is not the case when the RTC crystal's frequency is inaccurate.

32767d to 00000d more frequently than once a second if the source clock frequency is greater than 32.768 kHz and vice versa. When CNT_1 overflows from 32767d to 00000d, the microcontroller increments a second counter—CNT_2, for example. CNT_2 provides the count of the number of seconds elapsed since the system turned on.

To calibrate the system, the micro-

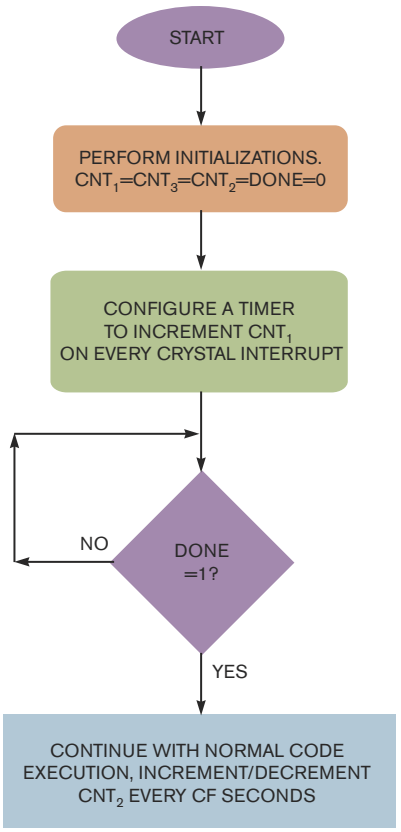

Figure 4 The main program of the microcontroller will increment or decrement CNT_2 every CF seconds apart from its normal functions.

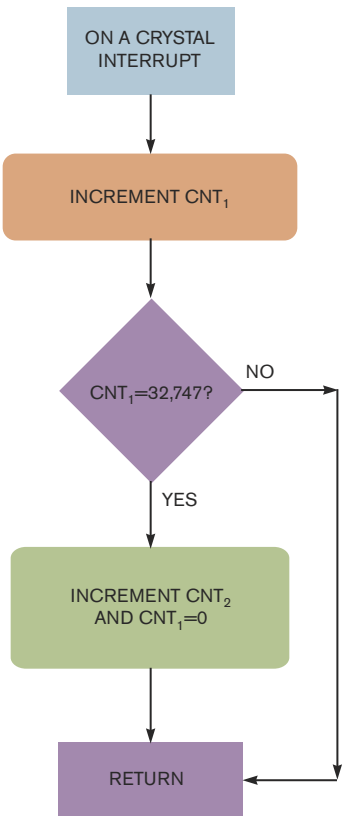

Figure 5 The algorithm increments CNT_1 in hardware every 1/32,768 seconds.

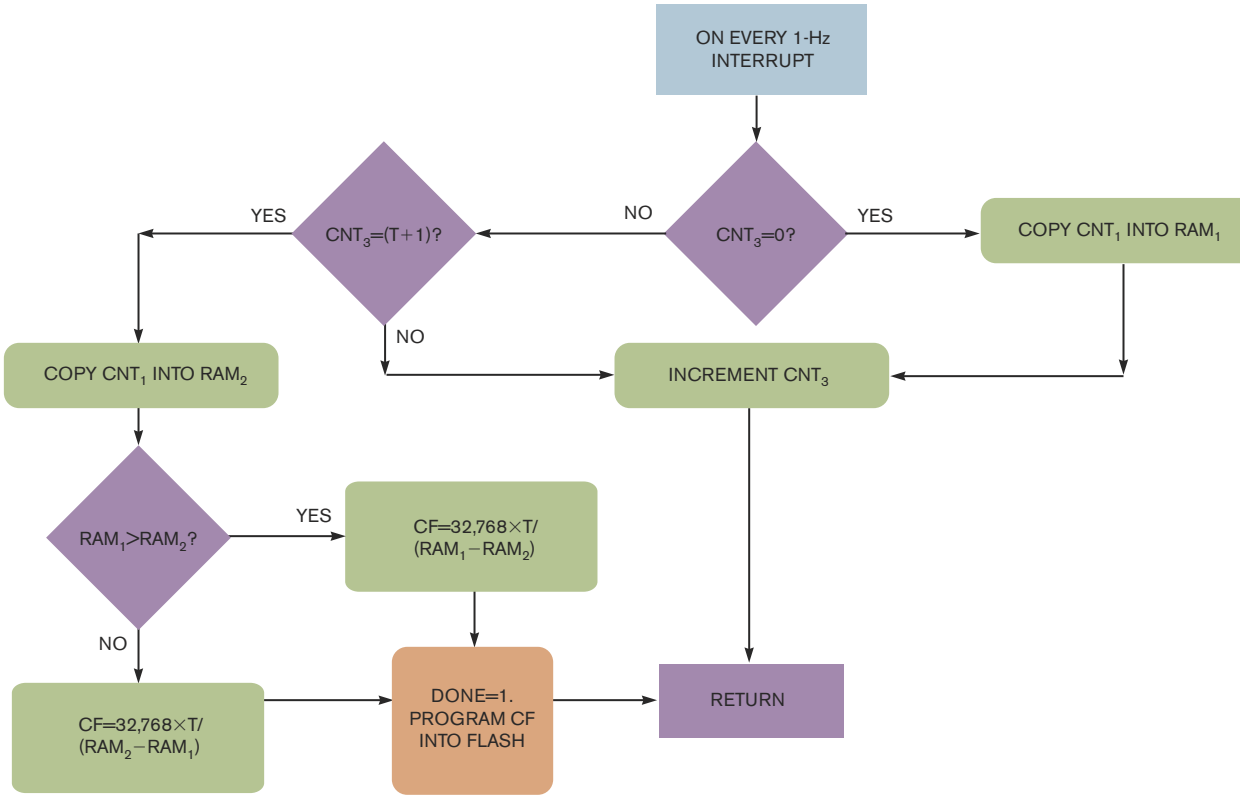

Figure 6 The microcontroller increments CNT_3 on each accurate, 1-Hz interrupt.

controller maintaining the time connects to the RTC crystal and to an accurate 1-Hz-interrupt source. This source can be generated using a combination of another microcontroller and an accurate and more costly RTC crystal. You can justify the use of an accurate RTC crystal because you must build this additional setup in small quantities just for calibration.

The first accurate 1-Hz interrupt can occur at any instant with respect to the power-on of the microcontroller you are calibrating. The value in CNT_1 on the first 1-Hz interrupt is VAL. If the RTC crystal is accurate, the value in CNT_1 at any of the 1-Hz interrupts would be VAL. This situation is true because CNT_1 would have overflowed and counted up to the same value each second. However, this scenario will not be the case when the RTC crystal's frequency is inaccurate (**Figure 3**). For this analysis, the observation time is T seconds. On the second and (T+1)th accurate 1-Hz interrupt, the microcontroller stores the contents of CNT_1. The microcontroller then calculates the calibration factor and

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stores it in its internal flash; if there is no way to write into the flash at runtime, the microcontroller can store the value in RAM and rely on the RTC's battery backup. Once this action is complete, the calibration algorithm can transfer the control to the main code that runs on the microcontroller.

In the flow charts of **figures 4**, **5**, and **6**, the microcontroller increments CNT_1 every 1/32,786 seconds and increments CNT_2 each time CNT_1 overflows from 32767d to 00000h. This counter is converted into hours, minutes, and seconds in software. The microcontroller increments CNT_3 on each accurate 1-Hz interrupt. At any given point, the value in CNT_3 is the number of seconds that elapsed since the first accurate 1-Hz interrupt plus one. E is the error in CNT_1 per increment of CNT_3. ERR_1 through ERR_T are the errors in CNT_1 after 1 through T seconds from the occurrence of the first accurate 1-Hz interrupt. Each interrupt corresponds to an increment in CNT_3. The total error in CNT_1 occurring in (T+1) seconds is $E_{TOTAL}=ERR_T$.

The purpose of this setup is to determine the average error in CNT_1 occurring on every 1-Hz interrupt through the increment count of CNT_3. You can also determine this error as follows: Error per second (E)=value of CNT_1 (when $CNT_3=2$)−value of CNT_1 (when $CNT_3=T+1$)/T. From the value of E, you can calculate the number of seconds after which a 1-second error would occur using the following **equation**: CF=32,768/E, where CF is the calibration factor. So, by incrementing or decrementing the value of CNT_2—that is, the seconds counter that the microcontroller maintains—every CF seconds, you should be able to achieve high accuracies. Alternatively, you can increment or decrement CNT_1 by CF counts every T seconds, which can yield higher accuracies because it avoids a division-rounding error. However, the former has been

adopted in this algorithm because CNT_1 was a nonmodifiable hardware counter in the experimental setup.

FLOW CHART AND PROCEDURE

Figures 4, **5**, and **6** describe the flow of the algorithm, which uses the following steps:

1. On each clock cycle of the inaccurate crystal, use a hardware-counter module to increment CNT_1.
2. Increment CNT_2 every time CNT_1 overflows from 32767d to 00000d.
3. On every accurate 1-Hz interrupt, increment CNT_3.
4. On the second accurate 1-Hz interrupt, copy the contents of CNT_1's initial value into a RAM location—say, RAM_1—and increment CNT_3. On subsequent accurate 1-Hz interrupts, increment CNT_3.
5. Once CNT_3 counts to T+1, where T is the observation interval, store the new value of CNT_1 into a RAM location—say, RAM_2.
6. Calculate the following **equations**: If $RAM_2 > RAM_1$, $E=(RAM_2-RAM_1)/T$; if $RAM_1 > RAM_2$, $E=(RAM_1-RAM_2)/T$; and $CF=32{,}768/E$.
7. Program the value of CF into the microcontroller flash. If necessary, use a glowing LED to indicate the completion of calibration.
8. The code running on the microcontroller must now increment the contents of CNT_2 by one every CF seconds if $RAM_1 > RAM_2$ or decrement the contents if $RAM_2 > RAM_1$.

SETUP AND RESULTS

The experimental setup to validate the RTC calibration algorithm comprises a microcontroller, M_1, and an inaccurate 32.768-kHz RTC crystal with an accuracy of 40 ppm. Another microcontroller, M_2, and a 32.768-kHz RTC crystal with an accuracy of 2 ppm generate the accurate 1-Hz source. The accurate 1-Hz clock from M_2 connects to an interruptible GPIO (general-purpose-I/O) pin of M_1. Observation times of powers of two ensure accurate division results when calculating the calibration factor. The calibration factor resides in M_1's flash memory. The main code on M_1 now compensates for the crystal frequency's inaccuracy based on this calibration factor, and M_1 was observed to achieve an RTC accuracy of approximately 2 ppm.

This approach allows you to manufacture the setup to generate the accurate 1-Hz interrupt in small quantities and use it across multiple boards. By increasing the observation time, you can achieve high accuracies. You can also use this algorithm to ascertain the exact parts-per-million accuracy rating of a crystal. Because most microcontrollers have sector-based flash, you can store the calibration code and the calibration factor in one sector and the user code in the remaining sectors.

This algorithm can achieve accurate timekeeping in a microcontroller-based RTC implementation. You must manually erase the calibration code on the microcontroller once the calibration completes; otherwise, you must permanently program the now-redundant calibration code into the flash. However, if you need to calibrate the microcontroller again due to a substantial change in temperature or aging, the presence of the calibration code is an advantage. You must connect the calibration setup to the device and disconnect it once the LED indicates that the calibration is complete. EDN

AUTHORS' BIOGRAPHIES

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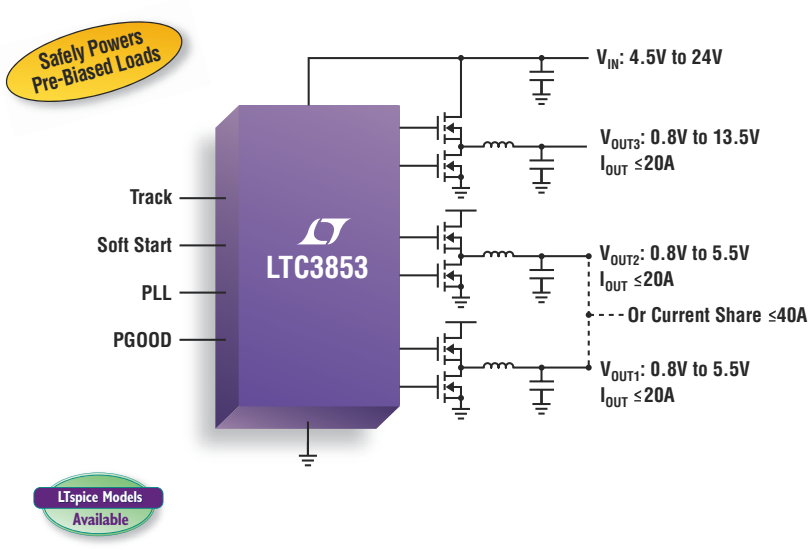
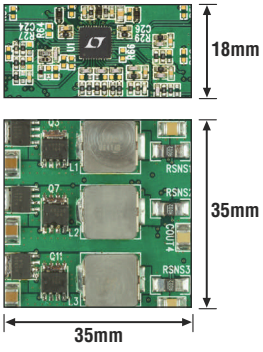


LTC3853 Demo Circuit



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LTC3879	1	4V to 38V		Y		$R_{DS(ON)}$	Y	Constant On-Time	3mm x 3mm QFN-16, MSOP-16E
LTC3850/-1/-2	2	4V to 30V	Y	Y	Y	DCR/R_{SENSE}	Y	250kHz to 750kHz	4mm x 4mm QFN-28, 4mm x 5mm QFN-28, Narrow SSOP-28
LTC3853	3	4.5V to 26V	Y	Y	Y	DCR/R_{SENSE}	Y	250kHz to 750kHz	6mm x 6mm QFN-40, 7mm x 7mm LQFP-48

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Precision tilt/fall detector consumes less than 1.5 mW

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

When you need to detect angular position related to Earth's gravity, you can use an Analog Devices (www.analog.com) three-axis MEMS (microelectromechanical-system) accelerometer. The ADXL335 has three analog outputs that correspond to the X, Y, and Z axes of an orthogonal coordinate system (**Reference 1**). Because the Z axis is perpendicular to the footprint, or base, of the MEMS IC's package surface, you can use the accelerometer to detect tilt if you mount it on a PCB (printed-circuit board) that's parallel to your product's base. The circuit in **Figure 1** lets you detect whether the tilt exceeds a preset limit. A digital output, in this example, drives an LED, but you can connect the signal to a microcontroller or another device.

When you orient the accelerometer IC horizontally relative to Earth, the LED is on. Whenever the Z axis of the device declines by a specific value, α_T, of the angle, α, from the vertical direction, the LED turns off. The voltage difference at the Z-axis output, Z_{OUT}, of the accelerometer, referenced to the power supply's midvoltage, $V_S/2$, is $V_{GZ}=V_G\cos\alpha$, where V_S is the power-supply voltage, V_{GZ} is the voltage at the Z_{OUT} pin, and V_G is the terrestrial full-scale voltage. When the power-supply voltage is 3V, the terrestrial full-scale voltage is either 300 or −300 mV, depending on whether you ori-

DIs Inside

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44 Circuit provides simpler power-supply-sequence testing

46 Inexpensive power switch includes submicrosecond circuit breaker

48 Create a DAC from a microcontroller's ADC

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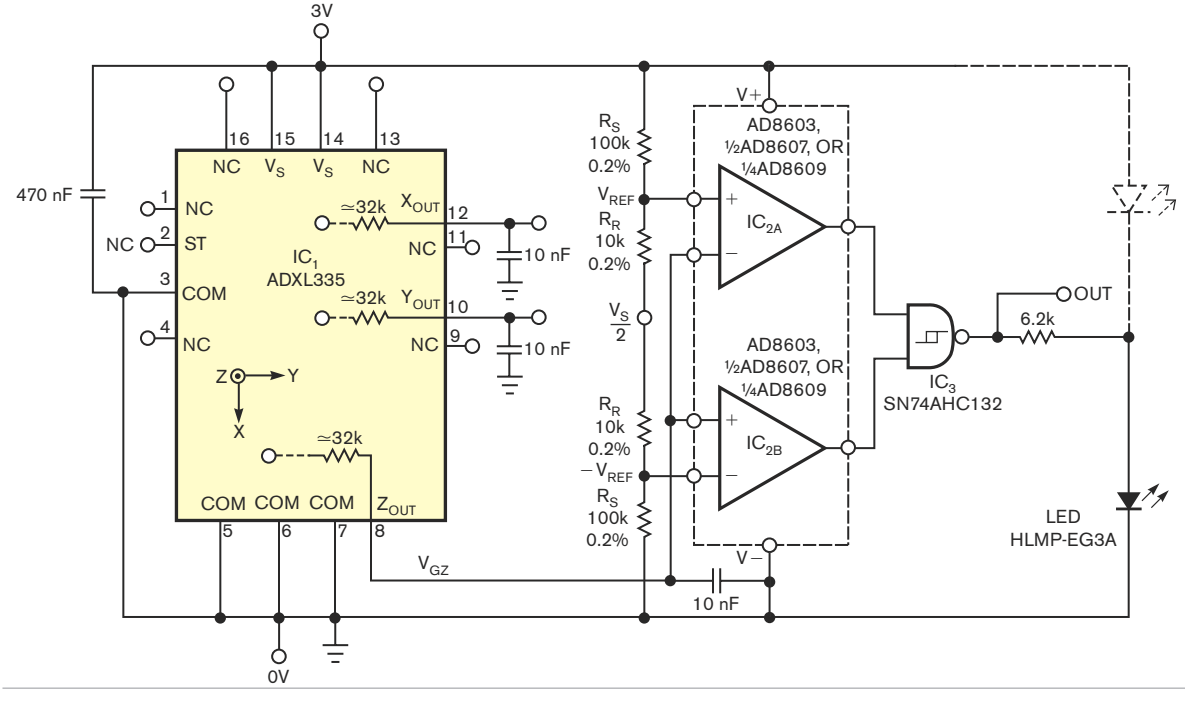

Figure 1 The tilt on MEMS accelerometer IC_1 produces a voltage, V_{GZ}. When compared with V_{REF} and $-V_{REF}$, V_{GZ} produces a digital output at the NAND gate.

ent the detector from the top down or from the bottom up. Op amp IC_2 compares the voltage at the Z_{OUT} pin to the reference voltage, V_{REF}. If the positive voltage at the Z_{OUT} pin is equal to or lower than the reference voltage, the output of IC_{2A} goes high, and the output of IC_{2B} remains high (**Reference 2**). Thus, the output of NAND gate IC_3 becomes low, and the LED turns off. You can calculate the threshold tilt angle, α_T, at which this action occurs from the **equation** $\cos\alpha_T=(V_{REF}/V_G)$.

Resistors R_S and R_R set the voltage reference to 136.36 mV. Thus, the threshold tilt angle is 62.96°. Similarly, when the negative voltage at the Z_{OUT} pin becomes lower in magnitude than the negative reference voltage, it indicates a tilt of 62.96° or more, the output of IC_{2B} goes high, and the LED (**Reference 3**) also turns off. Theoretically, you can choose any other threshold angle within the interval of 0 to 90°. The practical limits with the 10-nF filtering capacitor, however, are 21.23 and 86.10°. The probability of a short-term false detection is 8×10^{-5}. From the properties of the cosine function, the sensitivity of the tilt detector rises with rising tilt angle. To select another value of tilt within this interval, you calculate the appropriate reference voltage from the **equation** $\cos\alpha_T=(V_{REF}/V_G)$ and then change the value of the R_R resistors as necessary.

Gravity causes a voltage difference at the Z_{OUT} pin of IC_1. The circuit detects fall on the loss of this gravity-induced voltage difference within "free fall"—moving bodies with no acceleration other than that provided by gravity. If the circuit is fixed to such a body while the Z axis of IC_1 is pointing roughly vertically, the free fall manifests itself as almost fully disappearing within the 300- or −300-mV voltage excursion at Z_{OUT}. When the voltage remains close to the power supply's midvoltage, the voltage at Z_{OUT} is 1.5V. The threshold of detecting the free fall in this case is an apparent decrease in gravity to 0.4545g.

THE DETECTOR'S OPERATION IS VIRTUALLY INSENSITIVE TO POWER-SUPPLY VARIATIONS.

The probability that the noise's peak value will achieve this threshold value is practically zero for "heavy" bodies. The probability that the noise's peak value will achieve 0.0679g is fairly low, and it decreases vastly when you elevate the decision level. An apparent decrease in gravity within the free fall causes a low-to-high transition at the output of either IC_{2A} or IC_{2B}, depending on whether the Z axis is close to parallel or antiparallel to vertical. The outputs of both IC_{2A} and IC_{2B} remain at a high state. Thus, in both orientations, the output of the NAND gate goes low, and the LED turns off.

The sensitivity of IC_1 is essentially ratiometric. The resistive voltage divider R_S/R_R derives the positive and the negative reference voltages, which are inherently ratiometric. Thus, the detector's operation is virtually insensitive to power-supply variations. Note that the NAND gate has an internal Schmitt trigger at its inputs, and its logic output therefore fulfills industrial-grade requirements, including duration of the logic-state transitions of no more than 10 nsec regardless of the slope of the detected signal when crossing the threshold. If you need a complementary on/off indication, you can reconfigure the circuit by another position of the LED (dashed lines in **Figure 1**).EDN

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Reset an SOC only when power is ready

Goh Ban Hok, Lantiq Asia Pacific Pte Ltd, Singapore

An SOC (system on chip) normally requires two power supplies—one for the core supply and the other for the I/O. To properly power up the chip, you need to get one of the power supplies ready before the other, according to the SOC's power-sequence requirement. Normally, the core voltage must power up first, and the I/O voltage powers up second. Instead of direct control of the power supplies, you can control the system reset to achieve a similar goal. **Figure 1** shows the reset-conditioning circuit that can accomplish this task. In this circuit, the core voltage is 1.8V, and the I/O voltage is 3.3V. The reset-SOC signal produces a logic high when the core voltage gets ready before the I/O voltage. When the I/O voltage powers up first, the reset signal resets the SOC chip only after the core voltage powers up.

Comparator IC_1 monitors both voltages. It operates on the 3.3V I/O-supply voltage. Resistor R_2 and variable resistor R_1 form a voltage divider that lets you set the required voltage based on the core voltage. In this case, the reference voltage is 1.65V at Pin 3. Pushbutton switch S_1 provides a hard reset of the SOC.

In **Figure 2**, the core voltage (Trace A) powers up first, and the I/O voltage (Trace B) follows. Com-

LINEAR TECHNOLOGY

DESIGN NOTES

Using a Differential I/O Amplifier in Single-Ended Applications

Design Note DN473

Glen Brisebois

Introduction

Recent advances in low voltage silicon germanium and BiCMOS processes have allowed the design and production of very high speed amplifiers. Because the processes are low voltage, most of the amplifier designs have incorporated differential inputs and outputs to regain and maximize total output signal swing. Since many low-voltage applications are single-ended, the questions arise, "How can I use a differential I/O amplifier in a single-ended application?" and "What are the implications of such use?" This Design Note addresses some of the practical implications and demonstrates specific single-ended applications using the 3GHz gain-bandwidth LTC6406 differential I/O amplifier.

Background

A conventional op amp has two differential inputs and an output. The gain is nominally infinite, but control is maintained by virtue of feedback from the output to the negative "inverting" input. The output does not go to infinity, but rather the differential input is kept to zero (divided by infinity, as it were). The utility, variety and beauty of conventional op amp applications are well documented, yet still appear inexhaustible. Fully differential op amps have been less well explored.

Figure 1 shows a differential op amp with four feedback resistors. In this case the differential gain is still nominally infinite, and the inputs kept together by feedback, but this is not adequate to dictate the output voltages. The reason is that the common mode output voltage can be anywhere and still result in a "zero" differential input voltage because the feedback is symmetric. Therefore, for any fully differential I/O amplifier, there is always another control voltage to dictate the output common mode voltage. This is the purpose of the V_{OCM} pin, and explains why fully differential amplifiers are at least 5-pin devices (not including supply pins) rather than 4-pin devices. The differential gain equation is $V_{OUT(DM)} = V_{IN(DM)} \bullet R2/R1$. The common mode output voltage is forced internally to the voltage applied at V_{OCM}. One final observation is that there is no longer a single inverting input: both inputs are inverting and noninverting depending on which output is considered. For the purposes of circuit analysis, the inputs are labeled with "+" and "–" in the conventional manner and one output receives a dot, denoting it as the inverted output for the "+" input.

Anybody familiar with conventional op amps knows that noninverting applications have inherently high input impedance at the noninverting input, approaching GΩ or even TΩ. But in the case of the fully differential op amp in Figure 1, there is feedback to both inputs, so there is no high impedance node. Fortunately this difficulty can be overcome.

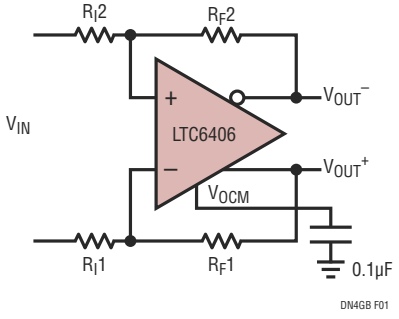

Figure 1. Fully Differential I/O Amplifier Showing Two Outputs and an Additional V_{OCM} Pin

Simple Single-Ended Connection of a Fully Differential Op amp

Figure 2 shows the LTC6406 connected as a single-ended op amp. Only one of the outputs has been fed back and only one of the inputs receives feedback. The other input is now high impedance. The LTC6406 works fine in this circuit and still provides a differential output. However, a simple thought experiment reveals one of the downsides

of this configuration. Imagine that all of the inputs and outputs are sitting at 1.2V, including V_{OCM}. Now imagine that the V_{OCM} pin is driven an additional 0.1V higher. The only output that can move is V_{OUT}^- because V_{OUT}^+ must remain equal to V_{IN}, so in order to move the common mode output higher by 100mV the amplifier has to move the V_{OUT}^- output a total of 200mV higher. That's a 200mV differential output shift due to a 100mV V_{OCM} shift. This illustrates the fact that single-ended feedback around a fully differential amplifier introduces a noise gain of two from the V_{OCM} pin to the "open" output. In order to avoid this noise, simply do not use that output, resulting in a fully single-ended application. Or, you can take the slight noise penalty and use both outputs.

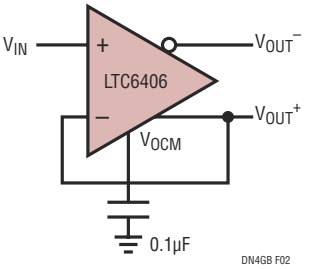

Figure 2. Feedback Is Single-Ended Only. This Circuit Is Stable, with a Hi-Z Input Like the Conventional Op Amp. The Closed Loop Output (V_{out}^+ in This Case) Is Low Noise. Output Is Best Taken Single-Ended from the Closed Loop Output, Providing a 3db Bandwidth Of 1.2ghz. The Open Loop Output (V_{out}^-) Has a Noise Gain Of Two From V_{ocm}, But Is Well Behaved to About 300mhz, Above Which It Has Significant Passband Ripple.

A Single-Ended Transimpedance Amplifier

Figure 3 shows the LTC6406 connected as a single-ended transimpedance amplifier with 20kΩ of transimpedance gain. The BF862 JFET buffers the LTC6406 input, drastically reducing the effects of its bipolar input transistor current noise. The V_{GS} of the JFET is now included as an offset, but this is typically 0.6V so the circuit still functions well on a 3V single supply and the offset can be dialed out with the 10k potentiometer. The time domain response is shown in Figure 4. Total output noise on 20MHz bandwidth measurements shows $0.8mV_{RMS}$ on V_{OUT}^+ and $1.1mV_{RMS}$ on V_{OUT}^-. Taken differentially, the transimpedance gain is 40kΩ.

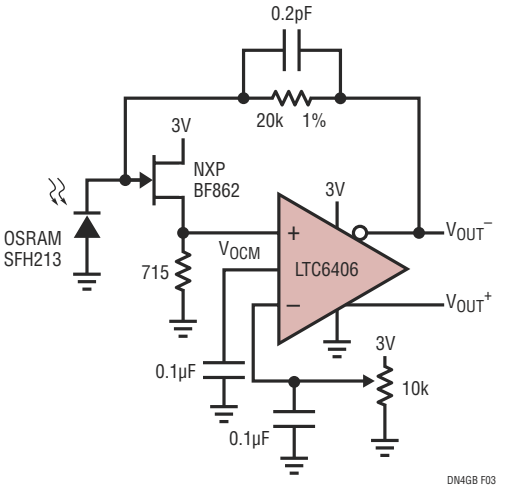

Figure 3. Transimpedance Amplifier. Ultralow Noise JFET Buffers the Current Noise of the Bipolar LTC6406 Input Trim the Pot for 0V Differential Output under No-Light Conditions.

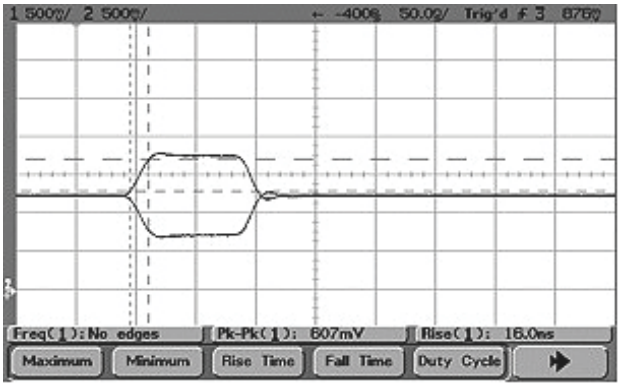

Figure 4. Time Domain Response of Circuit of Figure 3, Showing Both Outputs Each with 20kΩ of TIA Gain. Rise Time is 16ns, Indicating a 20MHz Bandwidth.

Conclusion

New families of fully differential op amps like the LTC6406 offer unprecedented bandwidths. Fortunately, these op amps can also function well in single-ended and 100% feedback applications.

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parator IC_1 remains inactive until the I/O voltage activates. When the I/O voltage turns on, comparator IC_1 and AND gate IC_{2A} operate. As the voltage at IC_1's Pin 2 is higher than that of Pin 3, the comparator produces a high at Pin 7, which pulls up through R_5.

The reset signal at IC_{2A}'s Pin 1 (Trace C) initially remains at zero and starts to charge capacitor C_1 to the I/O voltage through R_6. Depending on your application, you can adjust the RC time constant to suit your needs. The reset-in signal goes high after C_1 charges to the logic-high level, which produces a logic-high signal at Pin 3 (Trace D), resetting the SOC.

In **Figure 3**, the I/O voltage (Trace B) powers up first, and the core voltage (Trace A) follows. The core voltage powers up after the R_6/C_1 time constant. When the core voltage is 0V, the comparator voltage at Pin 3 is higher than it is at Pin 2. Thus, the comparator produces a logic low at Pin 7. Pin 1 of AND gate IC_{2A} remains high after the I/O voltage charges capacitor C_1. The reset-out signal remains at zero state because the core voltage is not yet present. When the core voltage comes up, the voltage at comparator IC_1's Pin 2 is higher than that of the threshold voltage at Pin 3. Thus, the comparator output's Pin 7 goes high. As reset remains high, the reset SOC of AND gate IC_2 goes high after a propagation delay. This action resets the SOC.

THE RESET-OUT SIGNAL REMAINS AT ZERO STATE BECAUSE THE CORE VOLTAGE IS NOT YET PRESENT.

In **Figure 4**, the I/O voltage (Trace B) powers on first, and the core voltage (Trace A) follows. This case is similar to that in **Figure 3** except that the core voltage powers up faster than the R_6/C_1 time constant. The comparator's IC_1 output, Pin 7, goes high when the core voltage turns on, and the voltage at Pin 2 crosses the threshold of 1.65V that resistor divider R_1/R_2 sets. However, the output reset's SOC signal goes high only when capacitor C_1 charges to the logic-high level. AND gate IC_{2A} then produces a high signal to reset the SOC. EDN

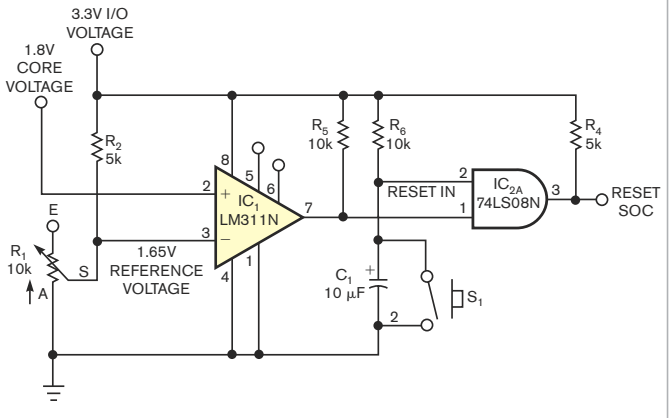

Figure 1 This circuit for reset conditioning uses a comparator and an AND gate.

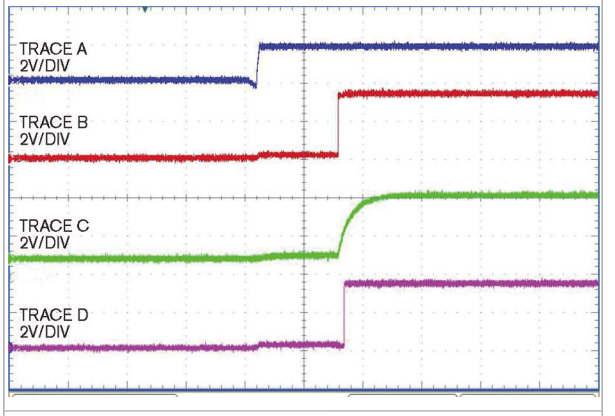

Figure 2 When the core voltage (Trace A) powers up before the I/O voltage (Trace B), the reset signal (Trace D) waits for the capacitor to charge.

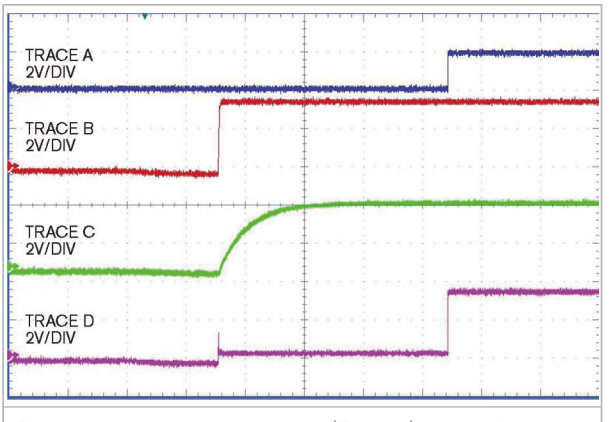

Figure 3 When the core voltage (Trace A) is late, the reset-SOC signal (Trace D) remains low.

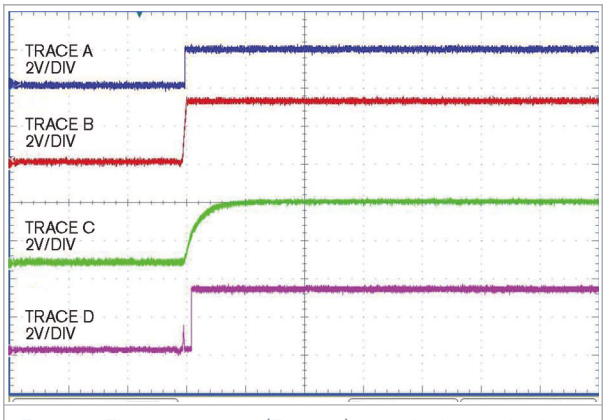

Figure 4 The reset signal (Trace D) goes high after both voltages come up and the capacitor charges.

Circuit provides simpler power-supply-sequence testing

Dan Karmann, DLK Engineering, Thornton, CO

A previous Design Idea (**Reference 1**) describes a three-IC control circuit for testing the power sequencing of an SOC (system on chip). Although that circuit lets you control the power-on sequence of two linear power supplies, it uses one eight-pin IC, two 14-pin ICs, several discrete components, and a DPDT (double-pole/double-throw) switch for the control. Replacing most of those components with an inexpensive, eight-pin microcontroller simplifies power-supply-sequencing control because the approach requires less wiring for component interconnections. The approach is also more versatile because it involves only simple changes to the controlling firmware. The simplicity and versatility come at approximately the same component cost.

A disadvantage of this circuit compared with the original is that it requires the appropriate firmware for the microcontroller, an Atmel (www.atmel.com) ATtiny13. However, free tools are available that let you develop and program the microcontroller. This Design Idea includes the source code for the operation of the sequencer in both Basic and C. You can download **Listing 1**, the code, from the online version of this Design Idea at www.edn.com/091203dia.

The demo version of the Bascom-AVR Basic compiler is fully functional and code-limited to 4 kbytes—four times the code space in the ATtiny13—and is freely downloadable for noncommercial development from MCS Electronics (www.mcselec.com). The WinAVR (winavr.sourceforge.net) tools used in this Design Idea use the GNU GCC C/C++, a fully functional, free open-source GNU GCC compiler. You can easily integrate the WinAVR compiler into the free IDE (integrated development) AVR Studio from Atmel. To program the Atmel microcontrollers, you can use free software tools through the microcontroller's six-pin SPI (serial-programming interface). You can download the easy-to-use, free PonyProg software from Lancos (www.lancos.com/prog.html) and also obtain the schematics for the programming circuits.

The circuit in **Figure 1**, like the circuit in **Reference 1**, includes two TPS75501 regulators, IC_2 and IC_3. This new circuit needs only IC_1, an eight-pin microcontroller; S_1, an SPST (single-pole/single throw) pushbutton switch to start the sequence; S_2, an SPST toggle switch, or a two-pin header with a jumper, to control the sequence order; and potentiometer R_3 to control the sequence delay. According to the firmware in **Listing 1**, pressing S_1 when S_2 is open causes the microcontroller to first turn on the 1.5V power supply and then turn on the 3.3V power supply following a delay that potentiometer R_3 controls. Pressing S_1 when switch S_2 is closed causes the microcontroller to first turn on the 3.3V power supply and then turn on the 1.5V power supply following a delay that potentiometer R_3 controls. As with the original Design Idea, a second press of S_1 causes the power supplies' turn-off to take place in the same sequence and with the same delay as their turn-on. This scenario provides an opportunity

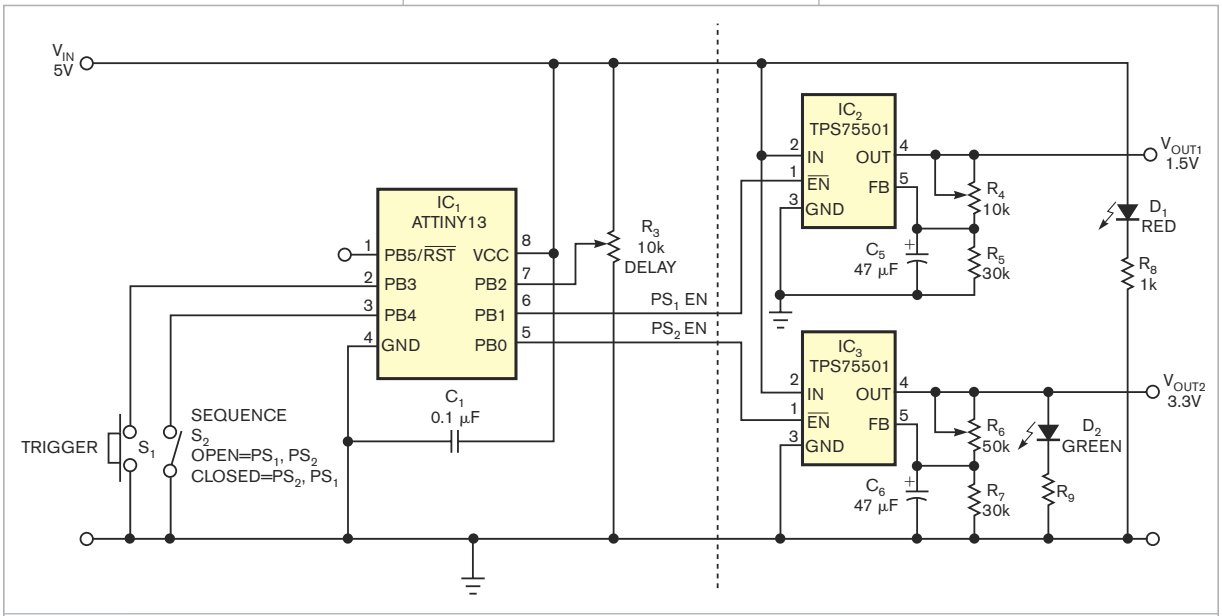

Figure 1 This circuit needs only an eight-pin microcontroller, an SPST pushbutton switch, an SPST toggle switch, and a potentiometer to control the sequence delay.

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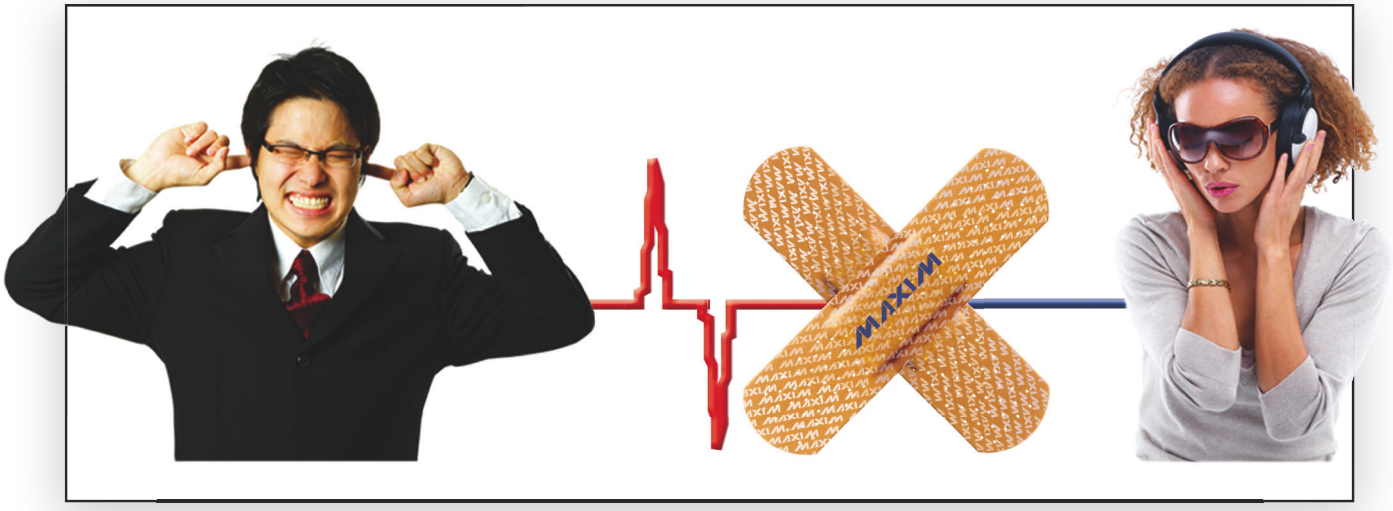

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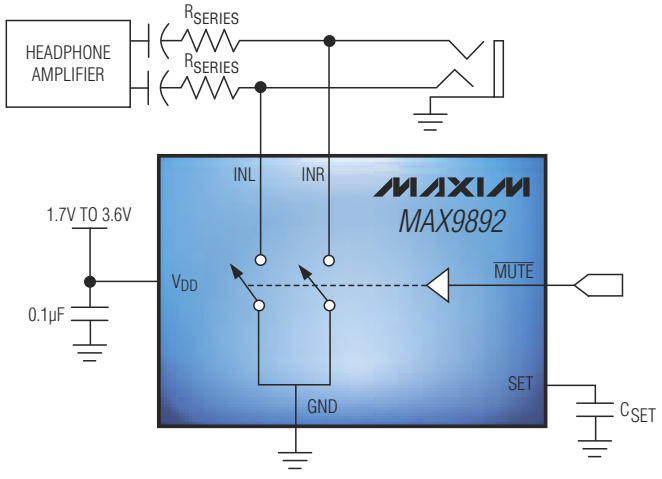

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The voltage level on Pin 7 of IC_1 determines the delay, under firmware control, between turning on or off the first and the second power supply. The microcontroller reads this delay voltage with its 10-bit ADC and uses the value to determine the delay according to the following **equation**: Delay=(V_{DELAY}/V_{CC})×1024×1 msec, where V_{DELAY} is the delay voltage. This **equation** yields a delay range from a few microseconds to a bit more than 1 second. As an example, if the delay-voltage value from R_3 is the midwiper value of 2.5V, the sequencing delay is approximately 512 msec: (2.5/5V)×1024×1 msec. The delay value is approximate because the microcontroller uses its internal 9.6-MHz RC oscillator to generate the timing with a simple firmware delay loop.

The code in **Listing 1** follows the original Design Idea in that a second press of trigger switch S_1 causes the power supplies to turn off in the same sequence and with the same delay with which they turn on. The **listing** includes a constant OFF_SEQUENCE that you can change to change the turn-off sequence with the second press of S_1 (**Figure 2**). This constant OFF_SEQUENCE is currently SEQUENCE_SAME to operate as the original Design Idea did, but if you set the OFF_SEQUENCE to SEQUENCE_REVERSE, the turn-off sequence will be in the opposite order of the turn-on sequence. Alternatively, if you set the constant OFF_SEQUENCE to SEQUENCE_NONE, both power supplies will turn off at once. This feature exemplifies the versatility of this follow-on Design Idea with a simple firmware change. Because the circuit uses only about half the code space in the ATtiny13, you could easily add other desired changes. Although this circuit uses an Atmel microcontroller, you can use almost any low-pin-count microcontroller with a built-in ADC. However, other brands may not have the readily available free development tools that exist for Atmel devices. EDN

REFERENCE

1 Ban Hok, Goh, "Circuit eases power-sequence testing," *EDN*, July 9, 2009, pg 50, www.edn.com/article/CA6668618.

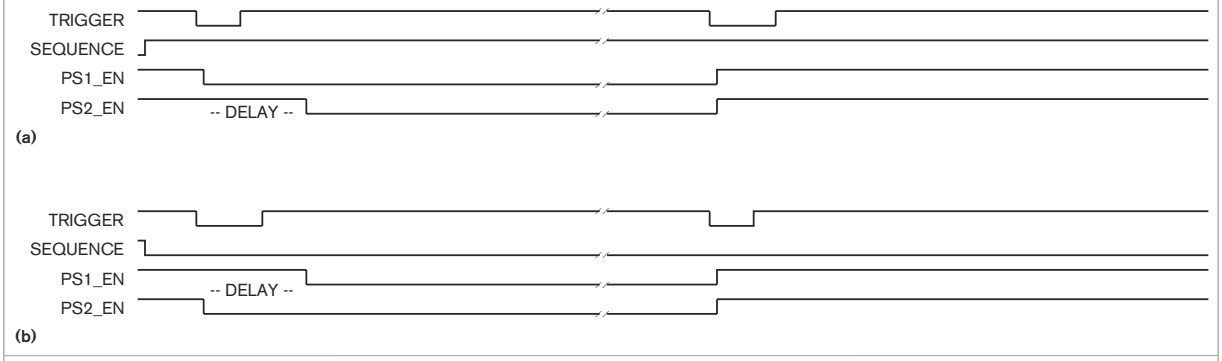

Figure 2 The timing sequence shows the power sequence for S_1 (a) and S_2 (b).

Inexpensive power switch includes submicrosecond circuit breaker

Anthony H Smith, Scitech, Bedfordshire, England

The circuit in **Figure 1** lets you switch high-voltage power to a grounded load with a low-voltage control signal. The circuit also functions as a submicrosecond circuit breaker that protects the power source against load faults. Power switches to the load when you apply a logic-level signal to the output control terminal. When the signal is lower than 0.7V, transistor Q_3 is off and the gate of P-channel MOSFET Q_4 pulls up to the positive supply through R_6, thus holding Q_4 off. During this off condition, the circuit's quiescent-current drain is 0A.

A 3 to 5V signal at the control terminal turns on Q_3, which pulls R_7 to 0V, providing gate drive for Q_4. The MOSFET now turns on and sources the load current, I_L, through sense resistor R_3 to the load. If R_3's and Q_4's on-resistances are smaller than the load resistance, the magnitude of the supply voltage, V_S, and the load resistance mainly determine the load current.

Under normal load conditions, the sense voltage developed across R_3 is too small to bias Q_1 on; thus, Q_1 and Q_2 are both off. If, however, the load current increases, the voltage across R_3 may become large enough to turn on Q_1. At that point, base current flows through R_4 to Q_1, and Q_1's collector current in turn provides base current for Q_2. As Q_2 turns on, it provides extra base drive for Q_1, and the two transistors rapidly latch in the on-state.

With Q_1 saturated, its collector pulls D_2's anode to the positive supply, which clamps Q_4's gate voltage to a diode drop below V_S. Without gate

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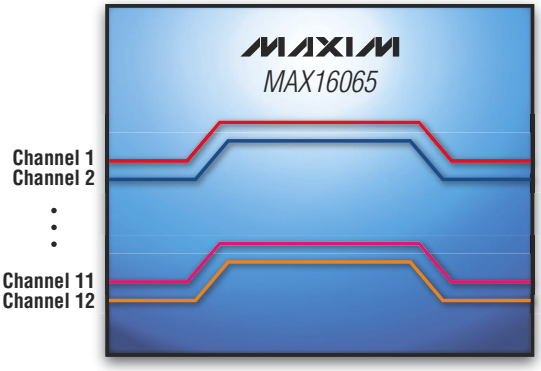

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drive, the MOSFET turns off, and I_L falls to 0A. With Q_1 and Q_2 both latched on, Q_4 remains off, which protects the power source from excessive load currents. You can reset the circuit breaker simply by taking the control signal low or by cycling the power. The resistance values in **Figure 1** are suitable for operation at supply voltages of 20 to 30V. Assuming that the transistors are suitably rated, the circuit can operate at much higher voltages, but you must scale the resistor values accordingly. Operation at a voltage as low as approximately 5V is also possible, but you may need to reduce the values of R_1 and R_5 to ensure proper drive for Q_1 and Q_2. Resistors R_6 and R_7 form a potential divider, which sets Q_4's gate-to-source voltage, V_{GS}, to a value large enough to enhance the MOSFET fully when Q_3 is turned on.

At low supply voltages, you may need to change the ratio of R_6 to R_7 to ensure that the gate-to-source voltage is large enough to provide adequate gate drive for Q_4. When the circuit is operating at high voltages, you may need small-signal diode D_1 to prevent reverse avalanche breakdown of Q_2's base-to-emitter junction when Q_3 is off. However, you can omit D_1 at low supply voltages, which are too small to cause avalanche breakdown.

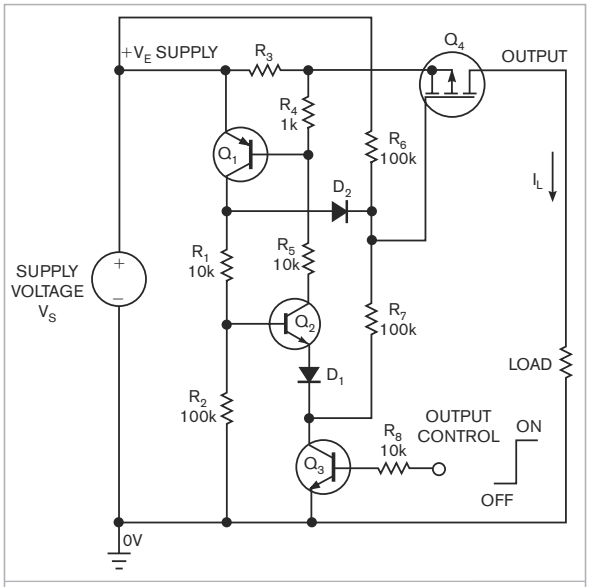

Figure 1 This inexpensive power switch incorporates a submicrosecond circuit breaker.

When selecting components, choose high-gain devices for the bipolar transistors and ensure that D_2 has low reverse-leakage current; avoid using a Schottky diode. In the off-state, each transistor has the full supply voltage across its collector-to-emitter or drain-to-source terminals, so ensure the maximum voltage ratings across these terminals are greater than the maximum supply voltage.

The circuit breaker trips at a load-current threshold: $I_{L(TRIP)} \simeq 0.5V/R_3$. For example, with a supply voltage of 24V and with R_3 having a value of 6.8Ω, a test circuit using the values in **Figure 1** trips at a load current of 70 mA. The actual trip point varies slightly with temperature and depends on the device you use for Q_1, so be prepared to adjust the value of R_3 to achieve the desired trip current.

In addition to providing a latching function, the positive feedback loop around Q_1 and Q_2 ensures that the circuit breaker responds quickly to an overload current. The actual trip time depends somewhat on the magnitude of the fault current. With a supply voltage of 24V and with R_3 having a value of 6.8Ω, the test circuit takes 6 μsec to trip at a fault current of 80 mA. However, increasing the fault current to 200 mA results in a trip time of just 500 nsec.

Capacitive loads, filament bulbs, and motors exhibit a large inrush current and could cause the circuit breaker to trip when the control signal goes high even though the normal, steady-state load current is below the trip threshold. If this scenario is likely to be a problem, consider connecting R_7 to a separate transistor so that you can independently control the circuit breaker and the power switch. This approach lets inrush current subside before enabling the circuit breaker. EDN

Create a DAC from a microcontroller's ADC

Vardan Antonyan, Glendale, CA

Few microcontrollers include a DAC. Although you can easily find an inexpensive DAC to control from your microcontroller, you can use unused peripherals instead of adding parts. Fortunately, you can convert a microcontroller's ADC channel along with a GPIO (general-purpose input/output) pin into a DAC. You can make a DAC by charging a capacitor to an analog level by driving it high. You can also discharge the capacitor by driving it low, or you can hold its voltage by tristating it (**Figure 1**). At first glance, this approach seems like a crude way to make a DAC. The technique becomes more plausible, however, when you use a PID (proportional-integral-derivative) algorithm and monitor the voltage with the microcontroller's ADC.

You can use the PID algorithm to compare the output voltage with the desired value and calculate the error. If the error value is zero, then the I/O control block tristates the GPIO pin. If the error signal is positive or negative, then the I/O control block turns the I/O pin to a high state to charge the capacitor or to a low state to discharge it. Your microcontroller code should load the error value into a timer to generate a timed pulse. The error-value sign determines the charge/discharge cycle, and its magnitude determines the duration of the pulse. Once the cycle is complete, you can set the I/O pin to a tristate mode, which holds the value.

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The algorithm can run as a software loop. You can call it based on another timer interrupt. To minimize the response time, make sure that this algorithm runs at the desired output value slightly longer than 2.2RC. You need the extra time to completely charge or discharge the capacitor through resistor R_1.

The DAC's resolution depends on several factors, the foremost of which is ADC resolution. The DAC's resolution never exceeds that of the ADC. Variable selection and timer resolution also affect DAC resolution. To implement a 10-bit DAC, you need a 16-bit timer and 16-bit variables for the PID algorithm. You can use a lower-resolution timer, but you must more frequently call the algorithm. That action results in longer settling times and higher CPU usage.

By adjusting the algorithm's PID variables, you can achieve surprisingly good output settling times with little change to the DAC's output after settling. The stability of the ADC's voltage reference limits temperature stability. Neither the temperature stability of R_1 and C_1 nor the leakage of C_1 has an adverse effect on the DAC's stability. The selection of R_1 and C_1 depends on the application, and you should select them based on settling time. For relatively slow-acting DACs, you can increase the update rate by running the algorithm faster than the 2.2RC period and using an 8-bit timer. To buffer the DAC output, use an op amp as a voltage follower or use a common emitter follower. You can use a noninverting amplifier to amplify the output and feed just a portion of it to the ADC through a voltage divider. EDN

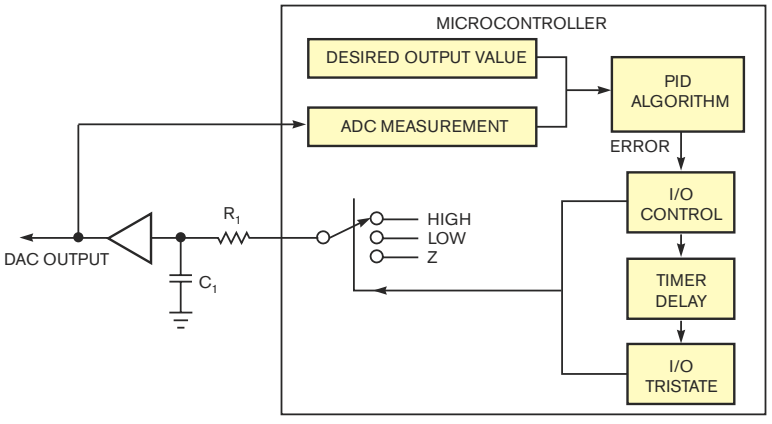

Figure 1 You can develop a PID algorithm to control pulse width and time, thus creating a DAC from a general-purpose I/O pin. Use the ADC as part of the feedback loop.

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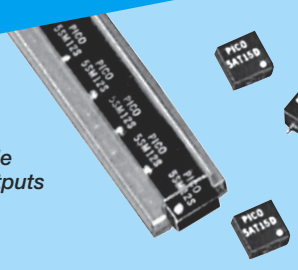

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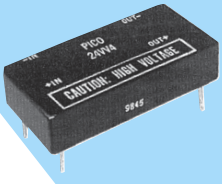

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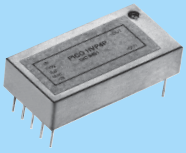

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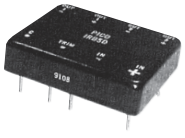

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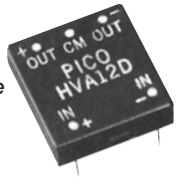

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LINKING DESIGN AND RESOURCES

Distributors respond to design trends

Although it appears that the design chain is streamlining, the opposite is true. Whereas engineers can cherry-pick among their suppliers' best technologies, integrating these devices into a cost-effective product design takes more time and effort.

"Designers used to be able to go to one source if they had questions or issues with a design," says Roy Vallee, chief executive officer of Avnet Inc (www.avnet.com). Suppliers used to offer a suite of products or technologies designed to work together. "Now, as suppliers focus on a single technology, [designers] have to go to their analog guy, memory guy, ASIC guy, and everyone else to solve a design problem," Vallee explains.

Although suppliers provide technical support for their own devices, they don't necessarily see a customer's entire design, says Michael Long, chief executive officer of Arrow Electronics Inc

(www.arrow.com). Designers could spend hours online or make a dozen phone calls to resolve a simple compatibility or integration issue. Along with shorter product lifetimes and tight OEM profit margins, "these forces are putting a lot of pressure on designers' cost and time," Vallee says.

Distributors are seizing this opportunity to showcase one of their core competencies: providing a one-stop shop for a variety of components and technologies. Even though the channel has cut personnel during the recession, distributors are retaining and investing in application engineers, Web tools, technical-training seminars, and other types of design assistance. "It's no longer about picking the best chip," says Jeff Hamilton (**photo**), director of marketing, design engineering, for distributor Newark (www.newark.com). "It's about making the best system decision."

A typical scenario, according to Digi-Key Corp (www.digikey.com), involves a design engineer who weighs the trade-offs between FPGAs and DSPs for a project. The designer hasn't used an FPGA, so a distributor's applications engineer helps the designer evaluate which product best meets the project's requirements.

Suppliers also benefit from a technically savvy channel. "We can add value by taking a Texas Instruments product, for example, targeted at the 4G [fourth-generation-communications] market and testing it in an application that needs wide bandwidth capability," says Hamilton. For more, visit www.edn.com/article/CA6704997.

—by Barb Jorgensen

GREEN UPDATE

WISCONSIN SIGNS ELECTRONICS-TAKE-BACK LAW

In late October, Wisconsin became the 20th state to sign a statewide recycling law that should affect the electronics supply chain. The comprehensive product-take-back legislation requires manufacturers of covered electronic devices sold in Wisconsin to register and recycle eligible devices. The law includes both performance standards based on the covered electronic devices and variable penalties for manufacturers that fail to meet those standards. As in many other states with product-take-back laws, the legislation sets collection goals based on each manufacturer's market share. The bill lists DVD players, VCRs (videocassette recorders), some telephones, cameras, PCs, printers, and TVs. The legislation will force electronics manufacturers to begin registering information on covered electronics in February 2010. For more on the legislation, see www.legis.state.wi.us/2009/data/acts/09enSB0107.pdf.**—SD**

OUTLOOK

DIGITAL-STB MARKET STILL STRONG

The digital-STB (set-top-box) market remains a "tremendous opportunity" for manufacturers and technology providers, according to In-Stat (www.in-stat.com). The research company reports that the overall digital-STB market grew from 37 million units in 2001 to nearly 190 million units in 2008, with product revenue at $18 billion. In 2009, In-Stat says, growth turned mixed across STB markets, with cable-STB shipments declining and satellite, IP (Internet Protocol), and digital-terrestrial segments continuing to see unit growth. "The transition from standard-definition to high-definition STBs will continue to provide STB vendors a solid growth opportunity," says Mike Paxton, an In-Stat analyst. "The integration of personal-video-recording capability is also creating growth opportunities." According to In-Stat, IP-STB shipments to telephone-company TV-service providers are slowing as subscriber growth matures and moderates.

In-Stat further notes that 2009 is a year of transition for digital-terrestrial STBs, as the completion in June of the analog switch-off in the United States created a "substantial bubble" of digital-terrestrial-STB shipments.**—SD**

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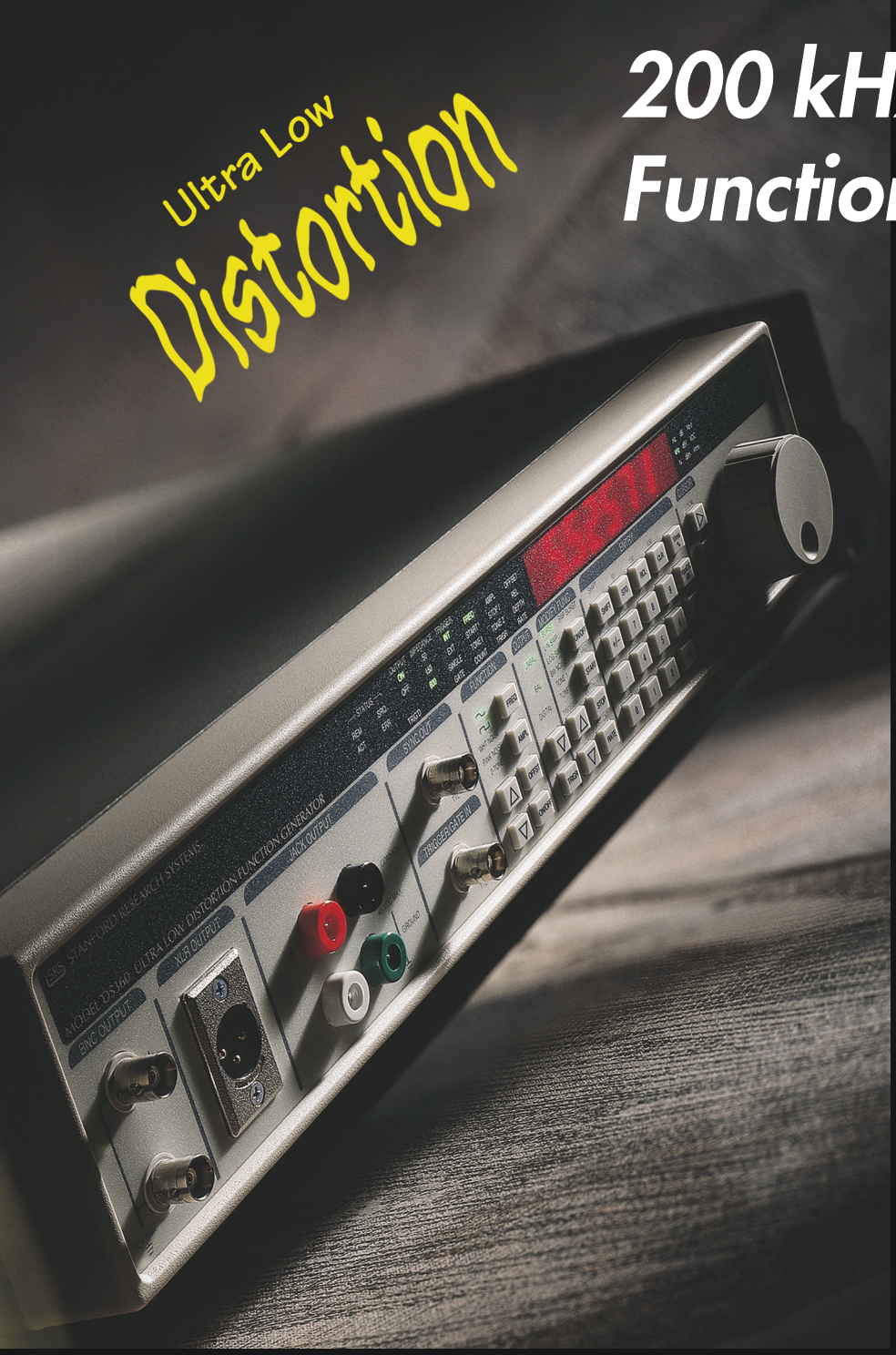

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productroundup

CONNECTORS

Power connectors use composite back shells for weight reduction

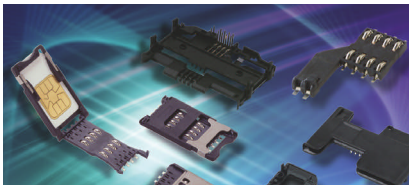
Targeting portable power systems and power-distribution boxes, the five-pole, 100A VEAM GRH-series connectors include rubber-covered coupling nuts, improving grip and durability, as well as a composite back shell, reducing weight and providing a streamlined profile. Features include finger-protected, set-screw termination-style contacts, allowing safe operation, wire installation, and field repair. The connectors also provide quarter-turn coupling; UL recognition; 100A continuous operation; and machined aluminum shells with a hard, black, anodized finish. Prices for the VEAM GRH connector series range from $230 to $250 (100) per mated pair.
ITT Interconnect Solutions, www.ittcannon.com

High-density interconnects have right-angle sockets

The high-density Searay open-pin field-interconnect family uses right-angle sockets, allowing connection to perpendicular and high-speed microbackplane applications. The device offers a four-row configuration with 200 contacts and a six-row configuration with 300 contacts. The system mates with the Searay surface-mount terminals with optional guideposts for blind mating and offers a choice of tin-lead or lead-free solder-charged termination. Available in a 1.27×1.27-mm grid array, the Searay high-density open-pin field-interconnect family costs 5 cents/pin (1000).
Samtec Inc, www.samtec.com

BGA-prototyping adapter has 500,000-spring-pin socket

The PA-BGA117C-P-S-01 prototyping adapter works with the SS-BGA117C-01 clamshell spring-pin ZIF socket, providing access to address and data lines and enabling IC swap-out. The adapter interfaces the 117-position, 0.075-in.-pitch BGA SMT-land pattern to a 0.1-in.-center PGA. Gold-plated, solder-tail, machined pins provide increased reliability when users plug the adapter into a receptacle or solder it to a PCB. The adapters optionally have wire-wrap pins, allowing designers to built prototypes on inexpensive wire-wrap panels. The clamshell ZIF socket has low-inductance spring pins with 500,000-insertion capability. The socket operates at 10-GHz bandwidth with less than 1-dB insertion loss. The adapter costs $190, and the clamshell spring-pin ZIF socket costs $1288 (10).
Ironwood Electronics, www.ironwoodelectronics.com



Smart-card connectors suit GPS and mobile-phone applications

Aiming at mobile-phone, point-of-sale, and GPS applications, the CCM01 and CCM02 smart-card connectors come in sealed, normally open card-detection switches, and a chamfered opening in the card-entry slot improves card guidance. The eight-contact CCM01 connector has a 100,000-cycle-minimum mechanical life. The eight-contact CCM02 connector has a 500,000-cycle-minimum mechanical life and provides an antipiracy system. Additional features include a 10N maximum card-insertion force and a 0.25 to 0.5N contact-force range. The connectors target use with full-sized ID1 cards, and prices range from 10 cents to $6, depending on type and quantity.
C&K Components, www.ck-components.com

Switchable graphics ICs improve battery life in notebook computers

The PS8271 HDMI/DVI 2-to-1 multiplexer, PS8321 DisplayPort 2-to-1 multiplexer, and PS8325 dual-mode cross-point switches enable switchable graphics implementations and improve battery life in notebook computers. The PS8321 multiplexer drives a DisplayPort video output from the active GPU, the PS8271 drives a DVI or an HDMI video output from the active GPU, and the PS8325 cross-point switch drives either a DisplayPort or an HDMI/DVI output from the active GPU. Available in a 7×7-mm QFN-48 package, the PS8271 costs $1.75 (100,000). The PS8321 comes in a 7×7-mm QFN-56 and costs $1.75, and the PS8325 comes in an 11×5-mm QFN-72 and costs $2.50.

Parade Technologies, www.paradetech.com

Notebook hard drive claims a 30% power reduction

The Scorpio Blue 640-Gbyte notebook hard drive comes in a 2.5-in. package with a 9.5-mm profile. Using 320-Gbyte-per-platter technology, the device packs 640 Gbytes into a standard two-disk form factor. The device consumes 30% less power than the vendor's previous Scorpio Blue drives. It sells for $149.

Western Digital, www.westerndigital.com

Display uses ECO mode for reduced power consumption

The 19-in. EA190M display, part of the vendor's MultiSync EA series, has a 5-to-4 standard aspect ratio at a 1280×1024-pixel native resolution. Features include 250-cd/m^2 brightness; 900-to-1 contrast ratio; 5-msec response; and a four-way ergonomic stand with a 110-mm adjustable height, pivot, tilt, and swivel. The device offers a two-step ECO mode, reducing power consumption, and a dynamic video mode with standard, text, movie, photo, and game presets. The display also provides space-saving down-firing multimedia speakers with a headphone jack. The display costs $259.

NEC Display Solutions of America, www.necdisplay.com

DisplayPort timing controls meet DDM specifications at 4M pixels

The DP627 and DP628 DisplayPort DDM (direct-drive-

monitor) timing controllers support 4M-pixel displays at 2560×1600-pixel WQXGA resolution and provide VESA DDM and VESA DisplayPort compatibility. The timing controllers display at a 10-bit depth. Suiting mid-range displays, the DPO627 features a four-lane DisplayPort input and a two-channel mini-LVDS output, supporting 1920×1200-pixel display resolution. Targeting high-end displays, the DP628 features a four-lane DisplayPort input and a four-channel mini-LVDS output, supporting 2560×1600-pixel display resolution. The timing controllers also include multichannel audio support through I^2C and S/PDIF output ports. The DP627 comes in an LQFP-128 and costs $4.50 (100,000); the DP628 comes in a DP628-172 and costs $7.

Parade Technologies,
www.paradetech.com

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Tanks a lot!

One of my company's products is an underwater acoustic sensor for use with an array of multiple hydrophones—electrical instruments for detecting or monitoring sound under water. The gain and phase-matching characteristics of these instruments are critically important, so we would every so often send production units to an outside lab to check these parameters.

On one occasion, an anomaly appeared in a customer-witnessed test that threatened to halt production and initiate an expensive recall. The problem was a phase difference between two units that far exceeded the allowable limit. It was especially puzzling that these same units matched well with another hydrophone but not with each other. Further testing then revealed that sometimes they did match each other, and sometimes they failed to match the third unit.

Testing occurred in a large, thick-walled cylinder mounted on end and extending through several floors of the building. Chain hoists lifted the massive lid, and wire bails attached to the lid mounted the sensors under test. Once the lid was replaced and tightly bolted, the cylinder was filled with water and pressurized to the equivalent of tremendous ocean depths.

During testing, acoustic projectors ensonified the cylinder—that is, filled it with acoustic radiation for observation and analysis—with sine-wave signals that varied over the frequency range of the sensors and recorded the sensors' outputs. An elaborate control system comprising projectors, reference hydrophones, and a computer controller eliminated sound reflecting off the chamber walls.

After several days of time-consuming testing, the results were more confusing than ever. There seemed to be no consistency to the failures. The only reliable observation was that the phase error varied with frequency as if there were a fixed time delay between the two sensors. We couldn't trace the time delay to any particular channel, sensor, or environmental condition. Once present, however, it remained until we changed the test setup.

The most reasonable explanation for this behavior was that the sensor pair was mounted at different heights within the test cylinder. A height difference of a few inches would account for the phase errors. We checked the sensor heights as they dangled from their mounting on the lid and found that they were identical. We tried watching the lid being lowered onto the cylinder, but observation during the last 6 inches was impossible due to the thickness of the stepped lid. We could find no explanation for a sensor-height difference.

As we were preparing for our final run, we milled about disconsolately, waiting for the equipment riggers to finish their job. It was our last chance to find the problem, but we had little hope that the last test would tell us anything. While waiting around, I happened to wander over to the test tank and leaned well over the railing to peer down inside the tank. What I saw shocked and then delighted me. The inside of the tank was not the smooth surface everyone had imagined but had various odd-shaped bumps projecting into the interior. These bumps enclosed the reference hydrophones, and we were deliberately adjusting the height of the hydrophones we were testing so that their acoustic centers were adjacent to a reference phone. There was nothing to prevent these knobs from snagging our somewhat-large sensor as we lowered it into the tank.

We quickly rerigged to the transverse set of wire bails so that our sensors would slide past the reference phone when we lowered it into the tank. We conducted the final test, and the problem was gone. EDN

James Casalegno is a senior systems engineer with Raytheon (Bristol, RI).

DANIEL VASCONCELLOS

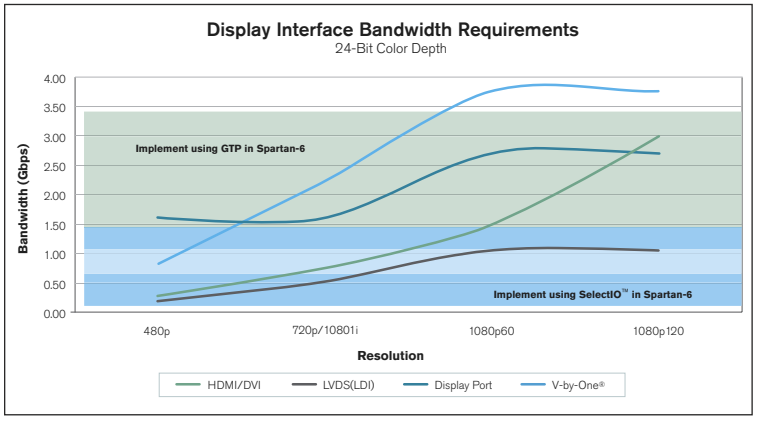
BY PATRICK DORSEY

Spartan-6 FPGAs — The Crystal Clear Advantage in Flat Panel TVs

In the age of the flat panel display, top TV manufacturers have to be extremely innovative. They not only have to figure out what advanced feature set they'll include in their next line of TVs, they must differentiate their TVs from a growing number of competitors, then get those TVs to market quickly. The most innovative OEMs have figured out that the secret to staying on top and keeping their edge in the TV market is to use low-cost Xilinx® Spartan® FPGAs instead of ASSPs. In January, Xilinx in partnership with distributor Tokyo Electron Device Ltd. (TED) will make the Spartan FPGA advantage even more clear with the release of its Spartan-6 FPGA Consumer Video Kit.

A few years ago, OEMs dealt with these design and market challenges by using one ASSP-based chip set across multiple product lines. By creating various software features that leverage these chips' internal processors, they could quickly, though not too resoundingly, distinguish one TV's feature set from the others in their product line. Unfortunately, a slew of competitors followed suit and began using the same ASSP chip sets. This limited differentiation, forced the big OEMs to drop price points, which significantly deteriorated profit margins.

By switching to Spartan FPGAs, OEMs can quickly enhance and optimize the full hardware functionality (as well as software and algorithms) of each product and integrate the functions of multiple chips into a single FPGA—eliminating the restrictions of an ASSP-based solution that only allows for limited modifications. This transition from a multichip ASSP-based system to a single-chip FPGA-based system saves power, space, cooling and improves overall system performance, while reducing overall bill of materials cost, and, above all, enabling end-product differentiation.



With integrated 3.125Gbps serial transceivers, the Spartan-6 family is ideally suited to support increasing line rate and bandwidth requirements of emerging TV standards.

What's more, the Spartan series' proven reliability and reprogrammability has helped OEMs drastically reduce defect rates and increase margins as well as consumer satisfaction, garnering their Spartan FPGA-based flat panel displays critical acclaim from editors and customers alike.

To build on this success in the consumer TV market and help OEMs and their suppliers leverage the integrated 3.125Gbps serial transceivers and other advanced features of Xilinx's new Spartan-6 family, in January Xilinx will announce the availability of the Spartan-6 FPGA Consumer Video Kit.

This easy-to-use and expandable kit will include a baseboard along with several FMC daughter cards, integrating soft IP logic blocks from Xilinx and its partner TED to support emerging and de facto high-speed display interfaces, including DisplayPort, V-by-One, high-speed LVDS and HDMI. The kit will streamline customer algorithm development on Spartan-6 based systems and give designers a jump on bringing differentiated products to the market quickly.

To learn more about the Spartan FPGA advantage, visit the Consumer Page at www.xilinx.com/consumer.

About the Author: Patrick Dorsey is the Sr. Director Product Management at Xilinx Inc. (San Jose, Calif.). Contact him at more_info@xilinx.com

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